Garda-5 Block Diagram

Project code: 91.4Q201.001
PCB P/N : 55.4Q201.XXX
REVISION : 06206-SA
(Hannstar, GCE)

-1-0426

CLK GEN.
ICS951413
(RTM865T-300/CY28RS400) 3

Mobile CPU
Yonah 478
4, 5

G792
20

AGTL+ 133/166MHz

ATI RC410ME
AGTL+ CPU I/F
SINGAL DDR2 CHANNEL
INTEGRATED GRAPHICS
LVDS/TVOUT/CRT
1 X4 PCIE SB I/F
6 X1 PCIE GPP I/F
Ver.:A13, 71.RC410.D0U
6,7,8,9,10

DDR2 x 2
11,12
533/667MHz

SVIDEO/COMP → TVOUT 14
LVDS → 14"WXGA+ LCD 13
RGB CRT → CRT 14
PCIE x 1 → Mini Card*1 802.11A/B/G 27
PCIE x 1 → New card 32 → PWR SW TPS2231 32

A-Link Express X4

ATI SB460
USB2.0 8Ports
SATA II (4 PORTS)
AZALIA HD AUDIO 1.0
AC97 2.3
ATA 66/100/133
LPC I/F
ACPI 1.2
INT RTC
PCI/PCI BDGE
Lab Ver. :A11, 71.SB460.A0U
Eng Ver. :A12, 71.SB460.B0U
15,16,17,18,19

Line In 31
MIC In 31
INT.MIC
Codec ALC883 30
AZALIA
INT.SPKR 31
OP AMP G1432Q 31
Line Out (SPDIF) 31
MAX4411
RJ11
MODEM MDC Card 22

PCI BUS
CARDBUS ENE CB1410 25
PCMCIA I/F
PWR SW TPS2211 26
PCMCIA SLOT Support TypeII 26
RICOH R5C832 1394 CardReader 28,29
1394 CONN 29
MS/MS Pro/xD/ MMC/SD/SDIO 6 in 1 29
Mini-PCI 802.11A/B/G 32
LAN Reltek10/100 RTL8100CL 23
TXFM 24
RJ45 24

LPC BUS
SIO NS87381 35
KBC ENE 3910 33
BIOS MX29LV800 36
LPC DEBUG CONN. 36
FIR 35
Touch Pad 34
INT. KB 34

SATA
PATA
USB 3 PORT 22
HDD 21
CDROM 21
MINI USB Blue-tooth 22

PCB STACKUP

TOP	
VCC	
S	
S	
GND	
BOTTOM	

SYSTEM DC/DC TPS51120 41

INPUTS	OUTPUTS
DCBATOUT	5V_S5 3D3V_S5

SYSTEM DC/DC TPS51124RGER 42

INPUTS	OUTPUTS
DCBATOUT	1D8V_S3 1D2V_S0
APL5312 120mA	
3D3V_S0	1D5V_CPU_S0 43
APL5332 1A	
3D3V_S0	1D5V_NEW_MINI_S0 43
APL5912 3A	
1D2V_S0	1D05V_S0 43
TPS51100 1A	
1D8V_S3	DDR_VREF_S3 DDR_VREF_S0 43
APL5308 300mA	
3D3V_S5	1D8V_S5 43

MAXIM CHARGER MAX8725 44

INPUTS	OUTPUTS
DCBATOUT	CHG_PWR 18V 4.0A UP+5V 5V 100mA

CPU DC/DC ISL6262 39,40

INPUTS	OUTPUTS
DCBATOUT	VCC_CORE_S0 0~1.3V 48A

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: BLOCK DIAGRAM
Size: A3 | Document Number: Garda-5 | Rev: -1
Date: Wednesday, April 26, 2006 | Sheet 1 of 46

USB	
Pair	Device
0	USB1
1	BT
2	USB2
3	NEW C
4	USB3
5	CCD
6	MINIC1
7	NC

PCI_CLK0	PCM
PCI_CLK1	IEEE1394
PCI_CLK2	LAN
PCI_CLK3	MINI
PCI_CLK4	KBC
PCI_CLK5	FWH
PCI_CLK6	SIO
PCI_CLK7	SPDIFOUT

PCI ROUTING TABLE

DEVICE	IDSEL	IRQ(Default)	REQ# / GNT#
MiniPCI	AD22	H	REQ#1/ GNT#1
R5C832	AD20	F : 1394 H : 6 in 1	REQ#3/ GNT#3
LAN(RTL8100CL)	AD17	E	REQ#2/ GNT#2
CARDBUS CB1410	AD16	G	REQ#0 / GNT#0
USB UHCI	AD29	A, B, C, D	
USB 2.0 EHCI	AD29	A	
DMI-to-PCI AC97 Modem AC97 Audio	AD30	B A	REQ#1 / GNT#1
LPC Bridge IDE SATA SMBus	AD31	A B B	
PCI Express	AD28	A, B, C, D	
Azalia Controller	AD27	A	

RESISTOR

Symbol name	Value	Tolerance (J: 5%, F: 1%, D: 0.5%, B: 0.1 %)	Rating 0402=> 1/16W, 25V 0603 => 1/16W, 75V 0805 => 1/10W, 100V	Size 2=>0402, 3=>0603, 5=>0805, 6=>1206, 0=>1210
10KR3	10K Ohm	If no letter, it means J: 5%	1/16W, 75V	0603
33D3R5	33.3 Ohm	If no letter, it means J: 5%	1/10W, 100V	0805
1KR3F	1K Ohm	F: 1%	1/16W, 75V	0603

The naming rule is value + R + size + tolerance
For the value, it can be read by the number before R. (R means resistor)
For the tolerance, it can be read from the last letter.
For the rating, we don't show on the symbol name.
For the size, R2=>0402, R3=>0603, R5=>0805,....

CAPACITOR

Symbol name	Value	Tolerance (J: +/-5, K: +/-10, M: +/-20, Z: +80/-20)	Rating (X5R / X7R < 80%, Y5V/Y5U/Z5U < 1/3)	Size 2=>0402, 3=>0603, 5=>0805, 6=>1206, 0=>1210
SCD1U10V2MX-1	0.1uF	M/X5R	10V	0402
SC10U6D3V5MX	10uF	M/X5R	6.3V	0805
SC2D2U16V5ZY	2.2uF	Z/Y5V	16V	0805

The naming rule is
Capacitor type + value + rating + size + tolerance + material
SCD1U10V2MX-1
SC=> SMT Ceremic, TC=> POS cap or SP cap
D1U => 0.1uF
10V => the voltage rating is 10V
2=> 0402, 3=>0603, 5=>0805
M=>tolerance J, K, M, Z
X=> X7R/X5R, Y=> Y5V
-1 => symbol version, nonsense to EE characteristic

History

```
==========================================================
2006/04/26 (-1 Modify)
1. page 27, change R8/R226 to 100 ohm due to power/email to dark.
2. page 15, change C286/C287 from 18pf to 15pf due to frequence shift(from -6.7 to 4ppm).
3. page 23, change C295/C294 from 15p to 12p due to frequence shift(from -23.3 to 7.9ppm).
4. EMI Solution for USB/MDC
        a. Change L23, L24, L31, L32 to "69.10084.071".
        b. del R353,R354,R356,R360,R445,R446.
        c. Change L1, L2 to "68.00331.011".
5. Page 44, change C12/C14 to 78.10699.43L due to 78.10699.42L Obsoleted.
==========================================================
2006/04/13 (-1 Modify)
1. Page 31, R447/R448 tp 33ohm.
2. Page 45, Add D4:83.P4SSM.0AM.
3. Page 44, Change C321 from 78.10492.4BL to 78.10224.2BL(1000P, 50V, K0603).
4. Page 23, change R209 from 5.6K to 5.37K.
5. Page 24, change XF1 from 68.68161.30A to 68.01201.30A.
6. Page 46, Mini card stand-off(銅柱) need to be changed from 34.4P401.001 to 34.4A907.001.
7. change 84.27002.L04 to 84.27002.F31.
==========================================================
2006/04/10 (-1 Modify)
1. Page 8, add "LVDS_DIGON" solution from ATI PA note.
2. Page 31, Add R to GND and serial R for U60 pin13/15.
==========================================================
2006/04/03 (SB Modify)
1. Page 40,  Dummy C593.
2. Page 44, Del C32.
3. Page 41, DCBATOUT_51120 change to DCBATOUT (Del G4,G5,G6,G7,G8)
4. Page 4/5, updae CPU symbol.
5. Page 15, Change X5 to same as X1 due to ME high limit issue, Cap. the same as X1 but should fine-tune.
6. Page 39/41/42, change "GAP-CLOSE-PWR" to 0 ohm PAD due to layout concern.
==========================================================
2006/03/31 (SB Modify)
1. Page 3, change R139 to bead and C211 to 2.2u for CRT Jitter.
2. Page 6, change R105 from 1.8K to 4.7K.
3. Page 8, change C165 to 2.2u for ATI recommend.
4. Page 8, SIV EDID_CLK/DAT issue, change RN53 to 4.7K.
5. Page 14, SIV RBG fail:
6. Page 15,
        a. PCIRST1#(1394) shoulder: Add 33 ohm @ SB.
        b. PLT_RST1# overshot : change R144 to 33ohm & R141 to 100P.
        c. Add 0ohm for RTC power for ATI recommend.
7. Page 40 , add 10U Cap.
8. Page 13/27, change Green LED4/LED5/LED1 to 83.00190.L70.
        (manual change yellow LED6/LED3/LED8/LED2 to 83.00190.S70).
9. EMI request:
        a. Page 13, USB_PP5,USB_PN5 add COMMON CHOKE.
        b. EC28,EC34,C208 add 0.1µCap.
        c. CLK48_ICH( near CLK GEN.),SB_CLK33_FWH(near R177) add 20p Cap..
==========================================================
2006/03/28 (SB Modify)
1. Page 14, change Q15/Q14 to 2N7002 for SIV CRT SMBus bug.
2. Page 15, Change C248/C261/C264/C263/C252 from 78.10491.4FL to 78.10523.5F1,
        and C262 from 78.10693.41L to 78.10623.51L.
3. Page 8, Add "LCDVDD_ON" PL 100K.
4. Page 41, change U7 to AO4406(84.04406.A37).
5. Page 33, KBC GPIO09 for 1394.
6. Page 33, add 1u Cap. for ENE ECRST# spec. 2ms.
7. Page 31, add audio popo noise solution.
8. Page 25, change C520 to 1U for "GBRST#".
9. Page 28, change "GBUS_GRST#_1" timing.
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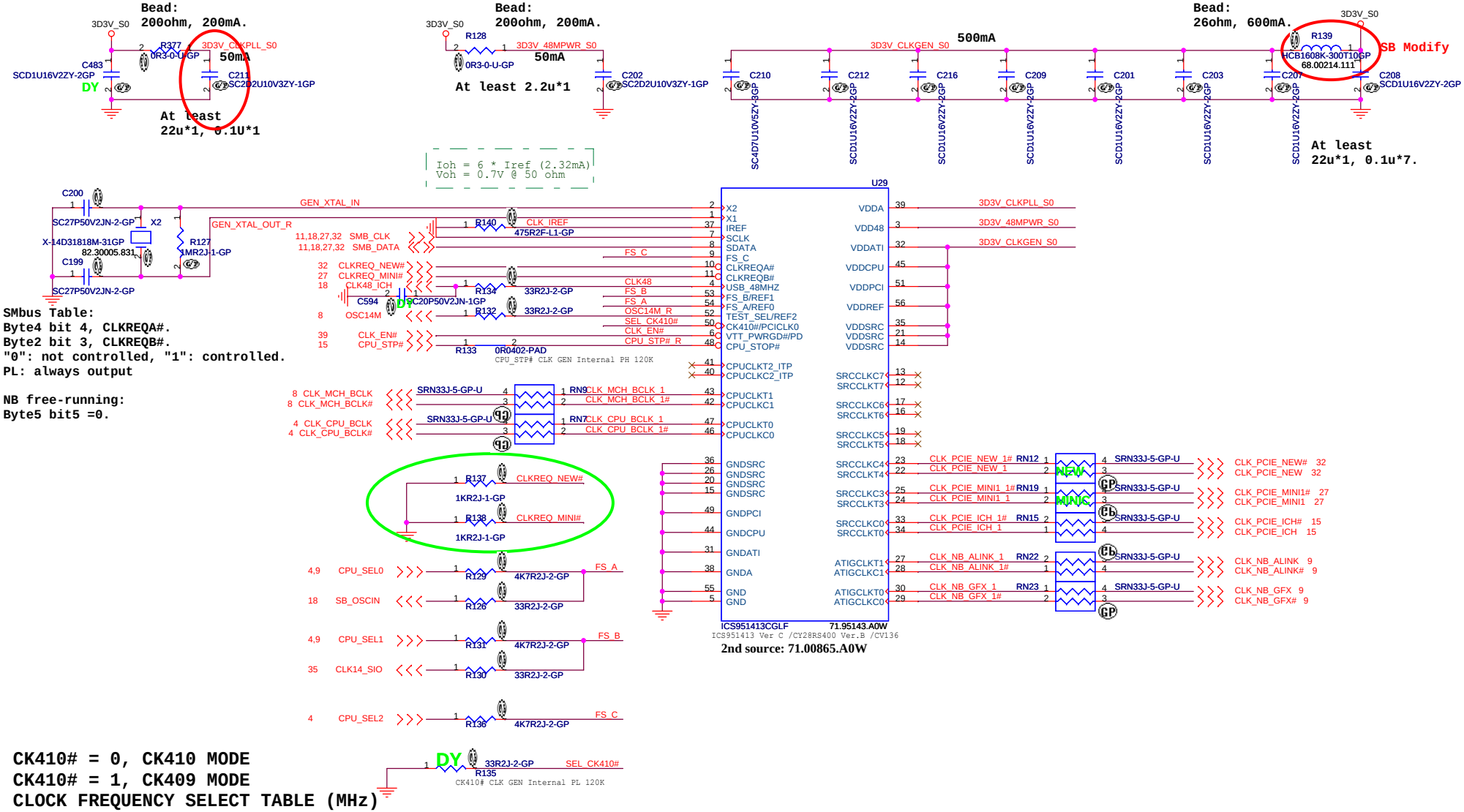
<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Reference

Size: A3 | Document Number: Garda-5 | Rev: -1

Date: Wednesday, April 26, 2006 | Sheet 2 of 46


Bead:
200ohm, 200mA.
3D3V_S0
R377
0R3-0-U-GP
3D3V_CLKPLL_S0
50mA
C483
SCD1U16V2ZY-2GP
DY
C211
SC2D2U10V3ZY-1GP
At least
22u*1, 0.1U*1
Bead:
200ohm, 200mA.
R128
0R3-0-U-GP
3D3V_48MPWR_S0
50mA
At least 2.2u*1
C202
SC2D2U10V3ZY-1GP
500mA
3D3V_CLKGEN_S0
C210
C212
C216
C209
C201
C203
C207
SC4D7U10V5ZY-3GP
SCD1U16V2ZY-2GP
Bead:
26ohm, 600mA.
R139
HCB1608K-300T10GP
68.00214.111
SB Modify
C208
SCD1U16V2ZY-2GP
At least
22u*1, 0.1u*7.
Ioh = 6 * Iref (2.32mA)
Voh = 0.7V @ 50 ohm
C200
SC27P50V2JN-2GP
X2
X-14D31818M-31GP
82.30005.831
R127
1MR2J-1-GP
C199
SC27P50V2JN-2GP
GEN_XTAL_IN
GEN_XTAL_OUT_R
SMbus Table:
Byte4 bit 4, CLKREQA#.
Byte2 bit 3, CLKREQB#.
"0": not controlled, "1": controlled.
PL: always output
NB free-running:
Byte5 bit5 =0.
11,18,27,32 SMB_CLK
11,18,27,32 SMB_DATA
R140
CLK_IREF
475R2F-L1-GP
32 CLKREQ_NEW#
27 CLKREQ_MINI#
18 CLK48_ICH
R134
33R2J-2-GP
CLK48
C594
SC20P50V2JN-1GP
FS_B
FS_A
8 OSC14M
R132
33R2J-2-GP
OSC14M_R
SEL_CK410#
39 CLK_EN#
15 CPU_STP#
CLK_EN#
CPU_STP# R
R133
0R0402-PAD
CPU_STP# CLK GEN Internal PH 120K
U29
X2
X1
IREF
SCLK
SDATA
FS_C
CLKREQA#
CLKREQB#
USB_48MHZ
FS_B/REF1
FS_A/REF0
TEST_SEL/REF2
CK410#/PCICLK0
VTT_PWRGD#/PD
CPU_STOP#
CPUCLKT2_ITP
CPUCLKC2_ITP
CPUCLKT1
CPUCLKC1
CPUCLKT0
CPUCLKC0
GNDSRC
GNDSRC
GNDSRC
GNDSRC
GNDPCI
GNDCPU
GNDATI
GNDA
GND
GND
VDDA
VDD48
VDDATI
VDDCPU
VDDPCI
VDDREF
VDDSRC
VDDSRC
VDDSRC
3D3V_CLKPLL_S0
3D3V_48MPWR_S0
3D3V_CLKGEN_S0
SRCCLKC7
SRCCLKT7
SRCCLKC6
SRCCLKT6
SRCCLKC5
SRCCLKT5
SRCCLKC4
SRCCLKT4
SRCCLKC3
SRCCLKT3
SRCCLKC0
SRCCLKT0
ATIGCLKT1
ATIGCLKC1
ATIGCLKT0
ATIGCLKC0
ICS951413CGLF
71.95143.A0W
ICS951413 Ver C /CY28RS400 Ver.B /CV136
2nd source: 71.00865.A0W
8 CLK_MCH_BCLK
8 CLK_MCH_BCLK#
SRN33J-5-GP-U
RN9
CLK_MCH_BCLK_1
CLK_MCH_BCLK_1#
4 CLK_CPU_BCLK
4 CLK_CPU_BCLK#
RN7
CLK_CPU_BCLK_1
CLK_CPU_BCLK_1#
R137
CLKREQ_NEW#
1KR2J-1-GP
R138
CLKREQ_MINI#
1KR2J-1-GP
4,9 CPU_SEL0
R129
4K7R2J-2-GP
FS_A
18 SB_OSCIN
R126
33R2J-2-GP
4,9 CPU_SEL1
R131
4K7R2J-2-GP
FS_B
35 CLK14_SIO
R130
33R2J-2-GP
4 CPU_SEL2
R136
4K7R2J-2-GP
FS_C
DY
R135
33R2J-2-GP
SEL_CK410#
CK410# CLK GEN Internal PL 120K
RN12
CLK_PCIE_NEW_1#
CLK_PCIE_NEW_1
RN19
CLK_PCIE_MINI1_1#
CLK_PCIE_MINI1_1
RN15
CLK_PCIE_ICH_1#
CLK_PCIE_ICH_1
RN22
CLK_NB_ALINK_1
CLK_NB_ALINK_1#
RN23
CLK_NB_GFX_1
CLK_NB_GFX_1#
SRN33J-5-GP-U
CLK_PCIE_NEW# 32
CLK_PCIE_NEW 32
CLK_PCIE_MINI1# 27
CLK_PCIE_MINI1 27
CLK_PCIE_ICH# 15
CLK_PCIE_ICH 15
CLK_NB_ALINK 9
CLK_NB_ALINK# 9
CLK_NB_GFX 9
CLK_NB_GFX# 9
CK410# = 0, CK410 MODE
CK410# = 1, CK409 MODE
CLOCK FREQUENCY SELECT TABLE (MHz)
FSC FSB FSA CPU SRC PCI REF
1 0 1 100 100 33 14.31
0 0 1 133 100 33 14.31
0 1 1 166 100 33 14.31
0 1 0 200 100 33 14.31
0 0 0 266 100 33 14.31
1 0 0 333 100 33 14.31
1 1 0 400 100 33 14.31
1 1 1 RESV 100 33 14.31
For Yonah Cerlon-M
For Yonah
CLK_PCIE_MINI1#
CLK_PCIE_MINI1
RN18
SRN49D9F-GP
CLK_PCIE_ICH
CLK_PCIE_ICH#
RN16
CLK_PCIE_NEW
CLK_PCIE_NEW#
RN11
CLK_NB_ALINK#
CLK_NB_ALINK
RN21
CLK_CPU_BCLK
CLK_CPU_BCLK#
RN8
CLK_MCH_BCLK
CLK_MCH_BCLK#
RN10
CLK_NB_GFX
CLK_NB_GFX#
RN24
<Variant Name>
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
Clock Generator -ICS951413
Size A3
Document Number
Garda-5
Rev SB
Date: Wednesday, April 26, 2006
Sheet 3 of 46

SB460 contains 400ohm inernal pull-up on CPU sideband signals.

A20M#
IGNNE#
INIT#
INTR/LIN0
NMI/LIN1
SMI#
STPCLK#

1D05V_S0
H_FERR# — R327 56R2J-4-GP
H_PWRGD — R330 330R2J-3-GP
H_BREQ#0 — R329 200R2J-L1-GP
H_DPSLP# — R326 200R2J-L1-GP
H_CPUSLP# — R331 200R2J-L1-GP

U53A

ADDR GROUP 0: H_A#[31..3] (A3# J4, A4# L4, A5# M3, A6# K5, A7# M1, A8# N2, A9# J1, A10# N3, A11# P5, A12# P2, A13# L1, A14# P4, A15# P1, A16# R1, ADSTB[0]# L2)

REQ[4..0]: H_REQ#0 K3, H_REQ#1 H2, H_REQ#2 K2, H_REQ#3 J3, H_REQ#4 L5

ADDR GROUP 1: H_A#17 Y2, H_A#18 U5, H_A#19 R3, H_A#20 W6, H_A#21 U4, H_A#22 Y5, H_A#23 U2, H_A#24 R4, H_A#25 T5, H_A#26 T3, H_A#27 W3, H_A#28 W5, H_A#29 Y4, H_A#30 W2, H_A#31 Y1, ADSTB[1]# V4

THERM: A20M# A6, FERR# A5, IGNNE# C4, THERMTRIP# C7

H CLK: STPCLK# D5, LINT0 C6, LINT1 B4, SMI# A3

RESERVED: RSVD[01] AA1, RSVD[02] AA4, RSVD[03] AB2, RSVD[04] AA3, RSVD[05] M4, RSVD[06] N5, RSVD[07] T2, RSVD[08] V3, RSVD[09] B2, RSVD[10] C3, RSVD[11] B25, RSVD[12] T22, RSVD[13] D2, RSVD[14] F6, RSVD[15] D3, RSVD[16] C1, RSVD[17] AF1, RSVD[18] D22, RSVD[19] C23, RSVD[20] C24

CONTROL: ADS# H1, BNR# E2, BPRI# G5, DEFER# H5, DRDY# F21, DBSY# E1, BR0# F1, IERR# D20, INIT# B3, LOCK# H4, RESET# B1, RS[0]# F3, RS[1]# F4, RS[2]# G3, TRDY# G2, HIT# G6, HITM# E4

XDP/ITP SIGNALS: BPM[0]# AD4, BPM[1]# AD3, BPM[2]# AD1, BPM[3]# AC4, PRDY# AC2, PREQ# AC1, TCK AC5, TDI AA6, TDO AB3, TMS AB5, TRST# AB6, DBR# C20

PROCHOT# D21, THERMDA A24, THERMDC A25

BCLK[0] A22, BCLK[1] A21

TP28 TPAD30

H_ADS# 6, H_BNR# 6, H_BPRI# 6, H_DEFER# 6, H_DRDY# 6, H_DBSY# 6, H_BREQ#0 6, H_IERR#, H_INIT# 15, H_LOCK# 6, H_CPURST# 6, H_RS#0, H_RS#1, H_RS#2, H_RS#[2..0] 6, H_TRDY# 6, H_HIT# 6, H_HITM# 6

XDP_BPM#0 TP47, XDP_BPM#1 TP49, XDP_BPM#2 TP50, XDP_BPM#3 TP48, XDP_BPM#4 TP46, XDP_BPM#5 TP51, XDP_TCK TP44, XDP_TDI TP37, XDP_TDO TP42, XDP_TMS TP38, XDP_TRST# TP45, XDP_DBRESET# TP20 (all TPAD30)

H_THERMDA — C84 SC2200P50V2KX-2GP — H_THERMDC

1D05V_S0 — R78 56R2J-4-GP

Place testpoint on H_IERR# with a GND 0.1" away

1D05V_S0 — R77 56R2J-4-GP — R76 DY 0R2J-2-GP

H_THERMDA 20, H_THERMDC 20, CPU_PROCHOT# 39, PM_THRMTRIP-I# 37

CLK_CPU_BCLK 3, CLK_CPU_BCLK# 3

TPAD30 TP41, TP39, TP43, TP40, TP32, TP31, TP35, TP36, TP22, TP21

TP34 TPAD30, TP26 TPAD30, TP27 TPAD30, TP52 TPAD30, TP25 TPAD30, TP24 TPAD30, TP23 TPAD30

BGA479-SKT6-GPU2
62.10079.001
2nd source: 62.10053.401

PM_THRMTRIP# should connect to ICH7 and Calistoga without T-ing (No stub)

H_D[63..0] 6

U53B

DATA GRP 0: H_D#0 E22, H_D#1 F24, H_D#2 E26, H_D#3 H22, H_D#4 F23, H_D#5 G25, H_D#6 E25, H_D#7 E23, H_D#8 K24, H_D#9 G24, H_D#10 J24, H_D#11 J23, H_D#12 H26, H_D#13 F26, H_D#14 K22, H_D#15 H25

DATA GRP 1: H_D#16 N22, H_D#17 K25, H_D#18 P26, H_D#19 R23, H_D#20 L25, H_D#21 L22, H_D#22 L23, H_D#23 M23, H_D#24 P25, H_D#25 P22, H_D#26 P23, H_D#27 T24, H_D#28 R24, H_D#29 L26, H_D#30 T25, H_D#31 N24

DATA GRP 2: H_D#32 AA23, H_D#33 AB24, H_D#34 V24, H_D#35 V26, H_D#36 W25, H_D#37 U23, H_D#38 U25, H_D#39 U22, H_D#40 AB25, H_D#41 W22, H_D#42 Y23, H_D#43 AA26, H_D#44 Y26, H_D#45 Y22, H_D#46 AC26, H_D#47 AA24

DATA GRP 3: H_D#48 AC22, H_D#49 AC23, H_D#50 AB22, H_D#51 AA21, H_D#52 AB21, H_D#53 AC25, H_D#54 AD20, H_D#55 AE22, H_D#56 AF23, H_D#57 AD24, H_D#58 AE21, H_D#59 AD21, H_D#60 AE25, H_D#61 AF25, H_D#62 AF22, H_D#63 AF26

6 H_DSTBN#0, 6 H_DSTBP#0, 6 H_DINV#0

H_DSTBN#2 6, H_DSTBP#2 6, H_DINV#2 6

6 H_DSTBN#1, 6 H_DSTBP#1, 6 H_DINV#1

H_DSTBN#3 6, H_DSTBP#3 6, H_DINV#3 6

MISC: GTLREF AD26, TEST1 C26, TEST2 D25, DPRSTP# E5, DPSLP# B5, DPWR# D24, PWRGOOD D6, SLP# D7, PSI# AE6

COMP[0] R26, COMP[1] U26, COMP[2] U1, COMP[3] V1

COMP0 R99 27D4R2F-L1-GP
COMP1 R102 54D9R2F-L1-GP
COMP2 R103 27D4R2F-L1-GP
COMP3 R104 54D9R2F-L1-GP

H_DPRSLP# 39, H_DPSLP# 15, H_DPWR# 6, H_PWRGD 15,37, H_CPUSLP# 18, PSI# 39

1D05V_S0 — R125 1KR2F-3-GP — CPU_GTLREF0 — R124 2KR2F-3-GP — C197 SC1KP16V2KX-GP

R80 DY 1KR2J-1-GP — R83 51R2F-2-GP

Layout Note: 0.5" max length.

3,9 CPU_SEL0, 3,9 CPU_SEL1, 3 CPU_SEL2

BSEL[0] B22, BSEL[1] B23, BSEL[2] C21

BGA479-SKT6-GPU2

Layout Note:
Comp0, 2 connect with Zo=27.4 ohm, make trace length shorter than 0.5" .
Comp1, 3 connect with Zo=55 ohm, make trace length shorter than 0.5" .

CPU on die PH 55 ohm

1D05V_S0
XDP_TDI — R107 150R2F-1-GP
XDP_TMS — R110 39D2R3F-2-GP
XDP_TDO — R112 DY 54D9R2F-L1-GP
H_CPURST# — R325 DY 220R2J-L2-GP

3D3V_S0
XDP_DBRESET# — R79 DY 150R2F-1-GP

XDP_TCK — R116 27D4R2F-L1-GP
XDP_TRST# — R115 680R3F-GP

All place within 2" to CPU

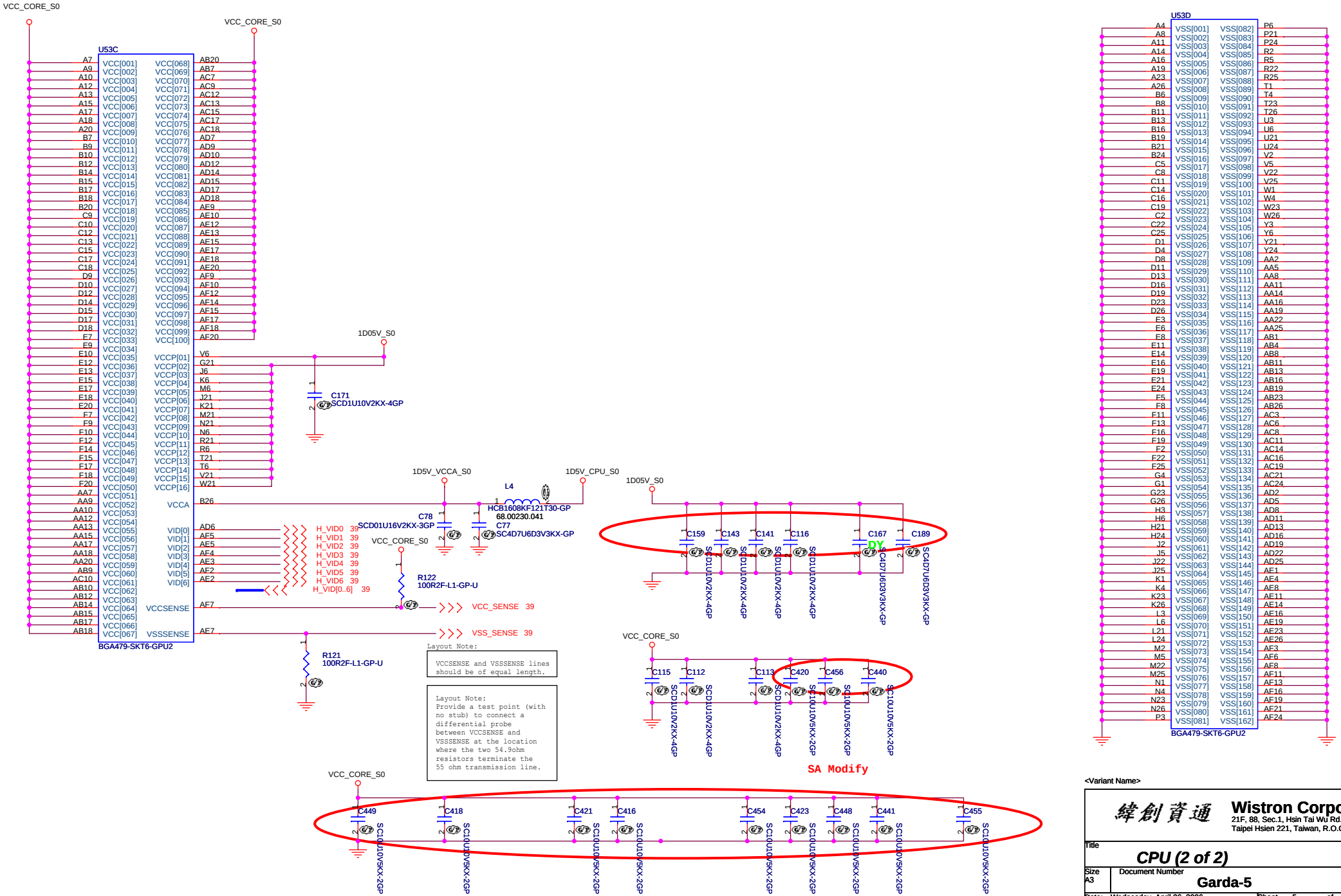
1D05V_S0 — R328 470R2J-2-GP — H_DPRSLP# — Q8 CH3904PT-GP — R71 470R2J-2-GP — PM_DPRSLPVR 15,39

3D3V_S0 — R378 10KR2J-3-GP

<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (1 of 2)
Size: A3 | Document Number: Garda-5 | Rev: SA
Date: Wednesday, April 26, 2006 | Sheet 4 of 46



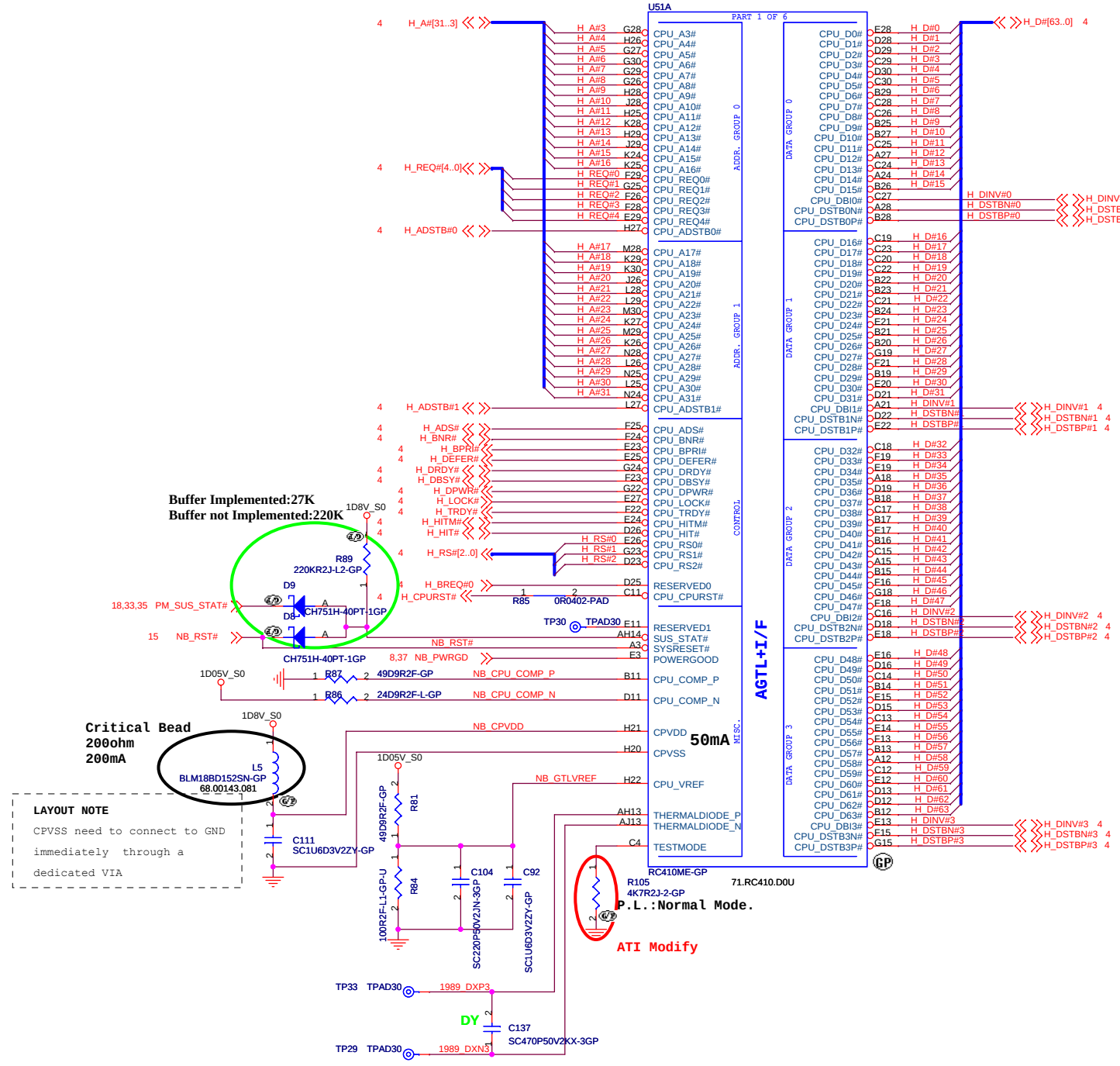
<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (2 of 2)

Size	Document Number	Rev
A3	Garda-5	SA

Date: Wednesday, April 26, 2006 Sheet 5 of 46



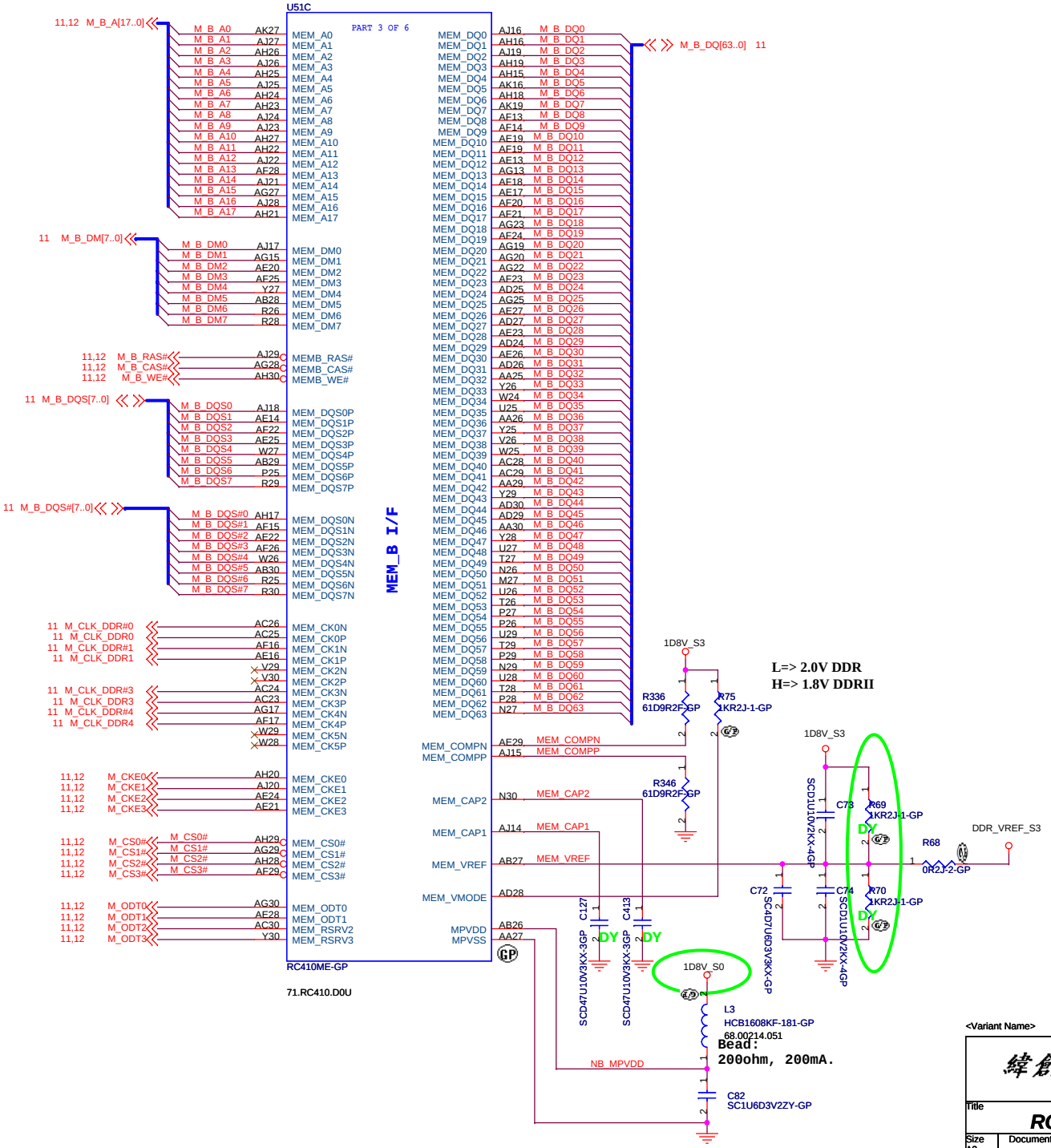
<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: RC410ME (1 of 5) Host I/F

Size	Document Number	Rev
A3	Garda-5	SB

Date: Wednesday, April 26, 2006 Sheet 6 of 46



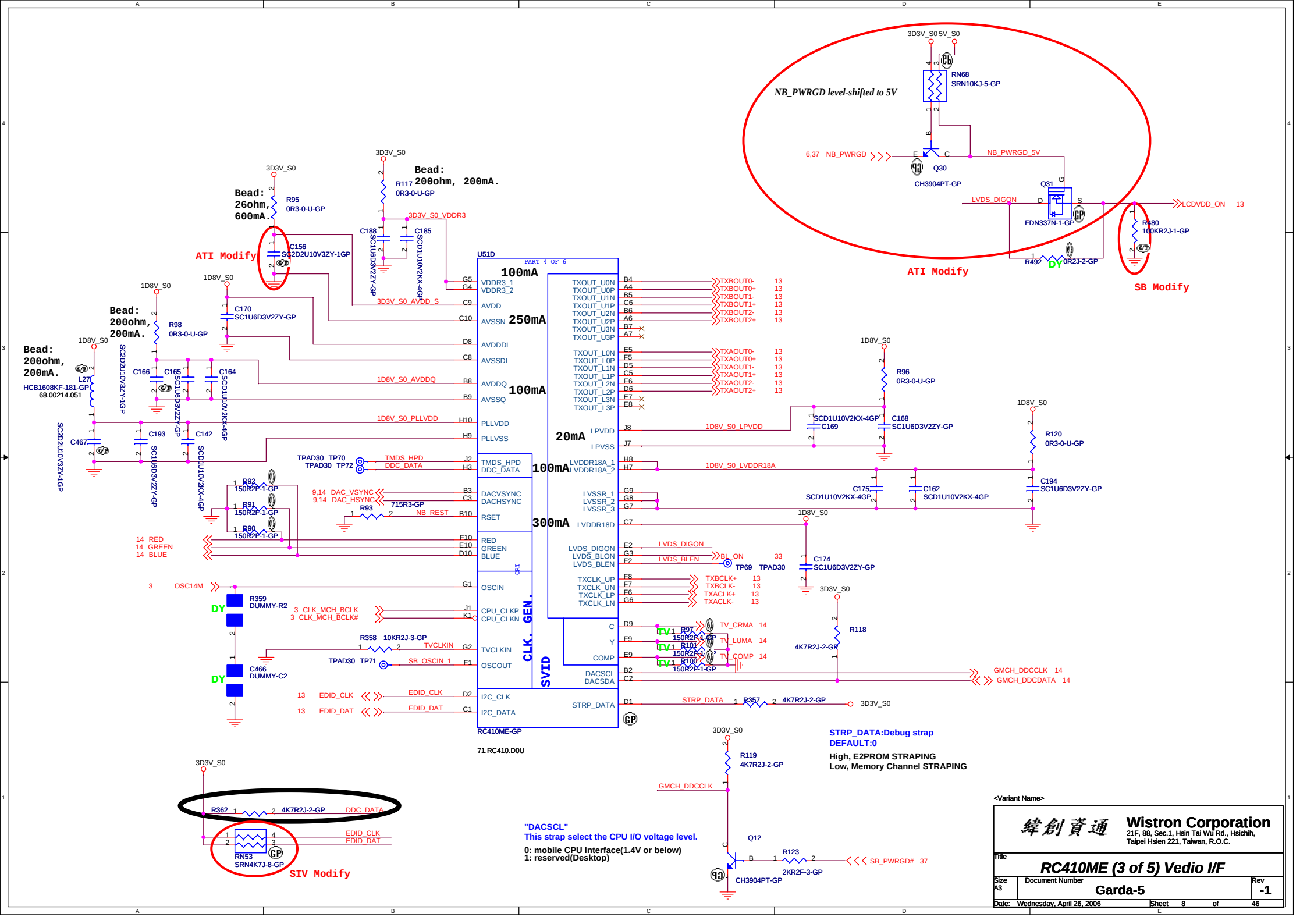
<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: RC410ME (2 of 5) Memory I/F

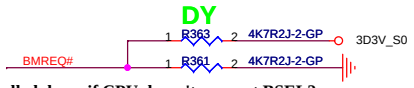
Size	Document Number	Rev
A3	Garda-5	SA

Date: Wednesday, April 26, 2006 Sheet 7 of 46

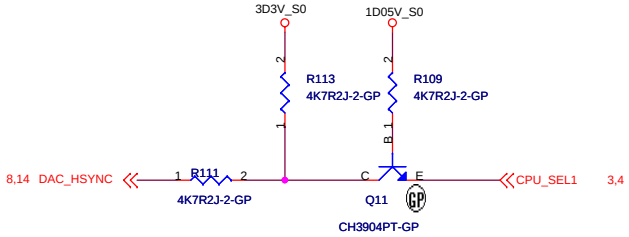

NB_PWRGD level-shifted to 5V
3D3V_S0 5V_S0
RN68
SRN10KJ-5-GP
6,37 NB_PWRGD
Q30
CH3904PT-GP
NB_PWRGD_5V
Q31
FDN337N-1-GP
LVDS_DIGON
LCDVDD_ON 13
R492
0R2J-2-GP
DY
R480
100KR2J-1-GP
ATI Modify
SB Modify
Bead: 26ohm, 600mA.
R95 0R3-0-U-GP
C156 SC2D2U10V3ZY-1GP
Bead: 200ohm, 200mA.
R117 0R3-0-U-GP
C188 SC1U6D3V2ZY-GP
C185 SCD1U10V2KX-4GP
3D3V_S0_VDDR3
Bead: 200ohm, 200mA.
R98 0R3-0-U-GP
C170 SC1U6D3V2ZY-GP
1D8V_S0
3D3V_S0_AVDD_S
1D8V_S0_AVDDQ
1D8V_S0_PLLVDD
Bead: 200ohm, 200mA.
L27 HCB1608KF-181-GP 68.00214.051
C166 SC2D2U10V3ZY-1GP
C165 SC1U6D3V2ZY-GP
C164 SCD1U10V2KX-4GP
C467
C193 SC1U6D3V2ZY-GP
C142 SCD1U10V2KX-4GP
U51D
PART 4 OF 6
100mA
250mA
100mA
20mA
100mA
300mA
VDDR3_1
VDDR3_2
AVDD
AVSSN
AVDDDI
AVSSDI
AVDDQ
AVSSQ
PLLVDD
PLLVSS
TMDS_HPD
DDC_DATA
DACVSYNC
DACHSYNC
RSET
RED
GREEN
BLUE
OSCIN
CPU_CLKP
CPU_CLKN
TVCLKIN
OSCOUT
I2C_CLK
I2C_DATA
LPVDD
LPVSS
LVDDR18A_1
LVDDR18A_2
LVSSR_1
LVSSR_2
LVSSR_3
LVDDR18D
LVDS_DIGON
LVDS_BLON
LVDS_BLEN
TXCLK_UP
TXCLK_UN
TXCLK_LP
TXCLK_LN
C
Y
COMP
DACSCL
DACSDA
STRP_DATA
CLK. GEN.
SVID
TXOUT_U0N
TXOUT_U0P
TXOUT_U1N
TXOUT_U1P
TXOUT_U2N
TXOUT_U2P
TXOUT_U3N
TXOUT_U3P
TXOUT_L0N
TXOUT_L0P
TXOUT_L1N
TXOUT_L1P
TXOUT_L2N
TXOUT_L2P
TXOUT_L3N
TXOUT_L3P
TXBOUT0-
TXBOUT0+
TXBOUT1-
TXBOUT1+
TXBOUT2-
TXBOUT2+
TXAOUT0-
TXAOUT0+
TXAOUT1-
TXAOUT1+
TXAOUT2-
TXAOUT2+
TPAD30 TP70
TPAD30 TP72
TMDS_HPD
DDC_DATA
9,14 DAC_VSYNC
9,14 DAC_HSYNC
715R3-GP
R93
NB_REST
R92 150R2F-1-GP
R91 150R2F-1-GP
R90 150R2F-1-GP
14 RED
14 GREEN
14 BLUE
3 OSC14M
R359 DUMMY-R2
DY
3 CLK_MCH_BCLK
3 CLK_MCH_BCLK#
R358 10KR2J-3-GP
TVCLKIN
TPAD30 TP71
SB_OSCIN_1
C466 DUMMY-C2
DY
13 EDID_CLK
13 EDID_DAT
EDID_CLK
EDID_DAT
R96 0R3-0-U-GP
SCD1U10V2KX-4GP
C169
C168 SC1U6D3V2ZY-GP
1D8V_S0_LPVDD
1D8V_S0_LVDDR18A
C175 SCD1U10V2KX-4GP
C162 SCD1U10V2KX-4GP
R120 0R3-0-U-GP
C194 SC1U6D3V2ZY-GP
C174 SC1U6D3V2ZY-GP
BL_ON 33
TP69 TPAD30
LVDS_DIGON
LVDS_BLEN
TXBCLK+ 13
TXBCLK- 13
TXACLK+ 13
TXACLK- 13
TV R97 150R2F-1-GP TV_CRMA 14
TV R101 150R2F-1-GP TV_LUMA 14
TV R100 150R2F-1-GP TV_COMP 14
R118 4K7R2J-2-GP
GMCH_DDCCLK 14
GMCH_DDCDATA 14
STRP_DATA
R357 4K7R2J-2-GP
RC410ME-GP
71.RC410.D0U
STRP_DATA:Debug strap
DEFAULT:0
High, E2PROM STRAPING
Low, Memory Channel STRAPING
R119 4K7R2J-2-GP
GMCH_DDCCLK
Q12
CH3904PT-GP
R123 2KR2F-3-GP
SB_PWRGD# 37
"DACSCL"
This strap select the CPU I/O voltage level.
0: mobile CPU Interface(1.4V or below)
1: reserved(Desktop)
R362 4K7R2J-2-GP
DDC_DATA
RN53 SRN4K7J-8-GP
EDID_CLK
EDID_DAT
SIV Modify
<Variant Name>
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
RC410ME (3 of 5) Vedio I/F
Size A3
Document Number Garda-5
Rev -1
Date: Wednesday, April 26, 2006
Sheet 8 of 46

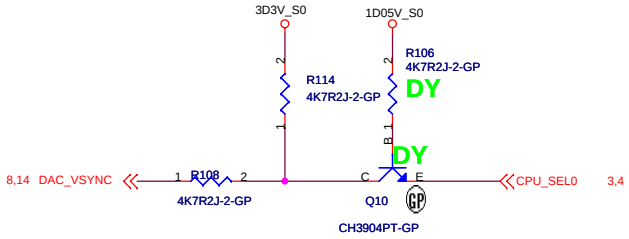
NB Strap pins

All pull-up and pull-down resistors are 4.7kohm.



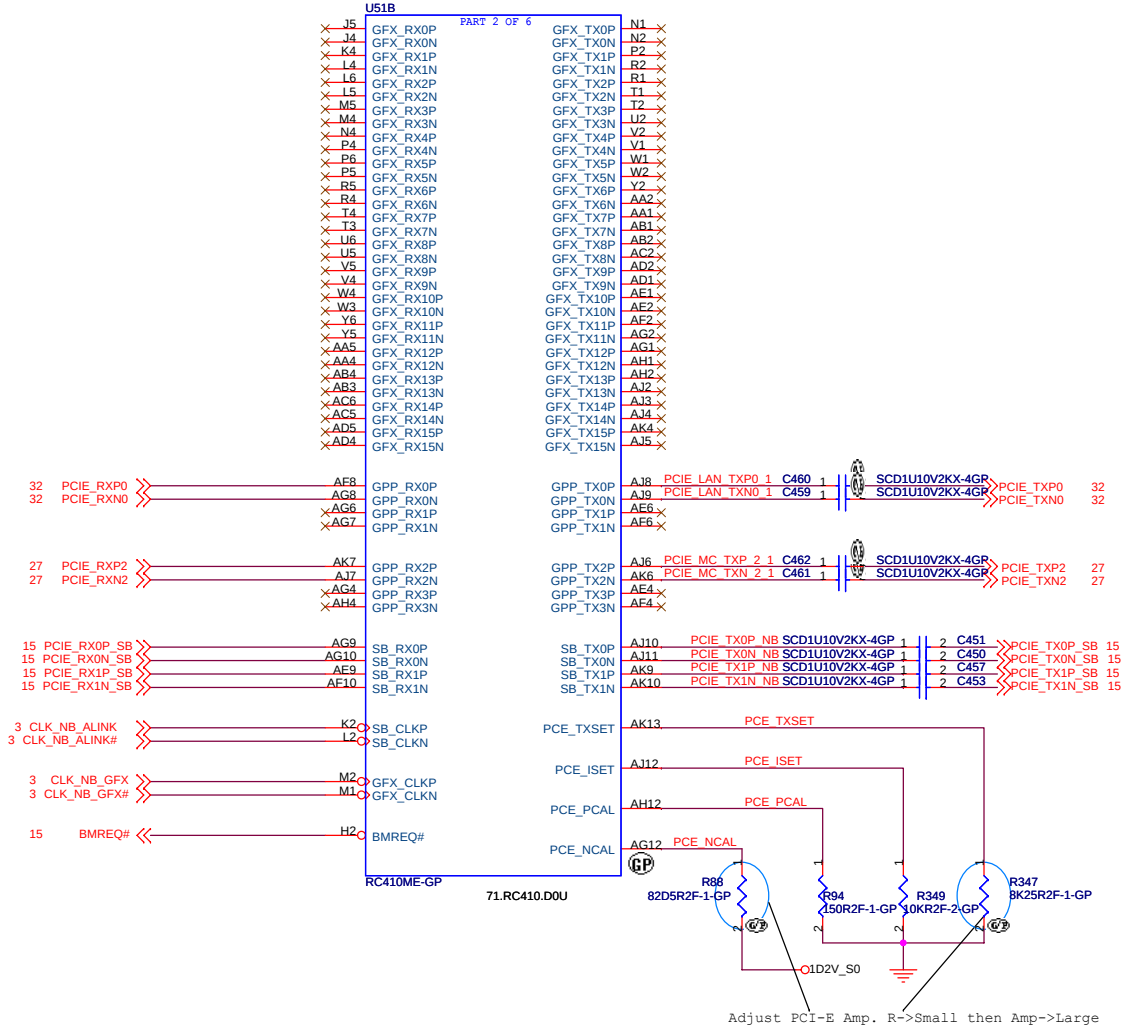
BMREQ# pulled down if CPU doesn't support BSEL2.





Select the FSB SPEED

BMREQ#	HSYNC	VSYNC	Freq.
0	0	0	100MHZ
0	0	1	133MHZ
0	1	0	------
0	1	1	166MHZ
1	0	0	100MHZ
1	0	1	100MHZ
1	1	0	------
1	1	1	------



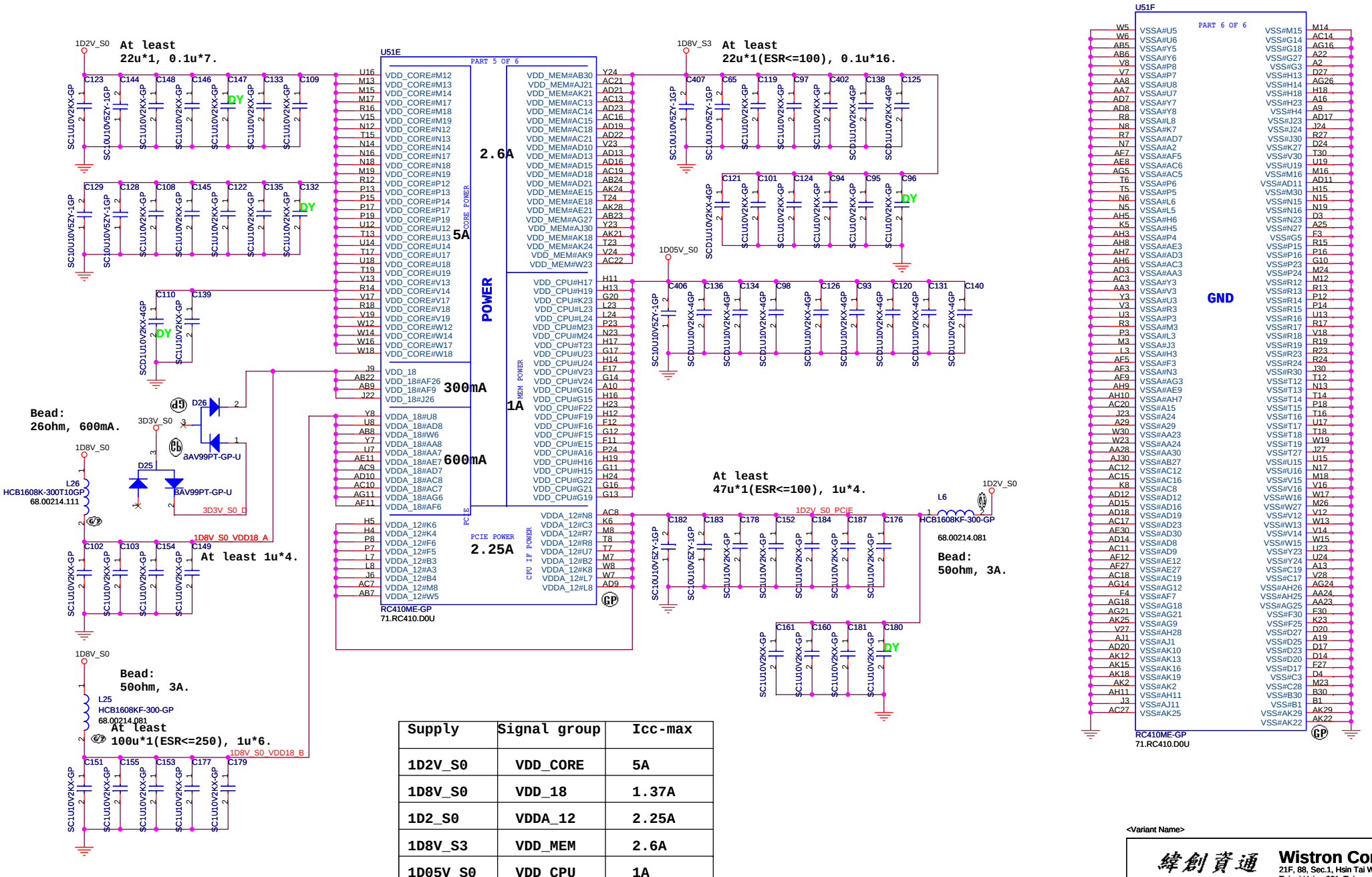
<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***RC410ME (4 of 5) PCI-E & Strap***

Size	Document Number	Rev
A3	Garda-5	SA

Date: Wednesday, April 26, 2006 Sheet 9 of 46



Supply	Signal group	Icc-max
1D2V_S0	VDD_CORE	5A
1D8V_S0	VDD_18	1.37A
1D2_S0	VDDA_12	2.25A
1D8V_S3	VDD_MEM	2.6A
1D05V_S0	VDD_CPU	1A

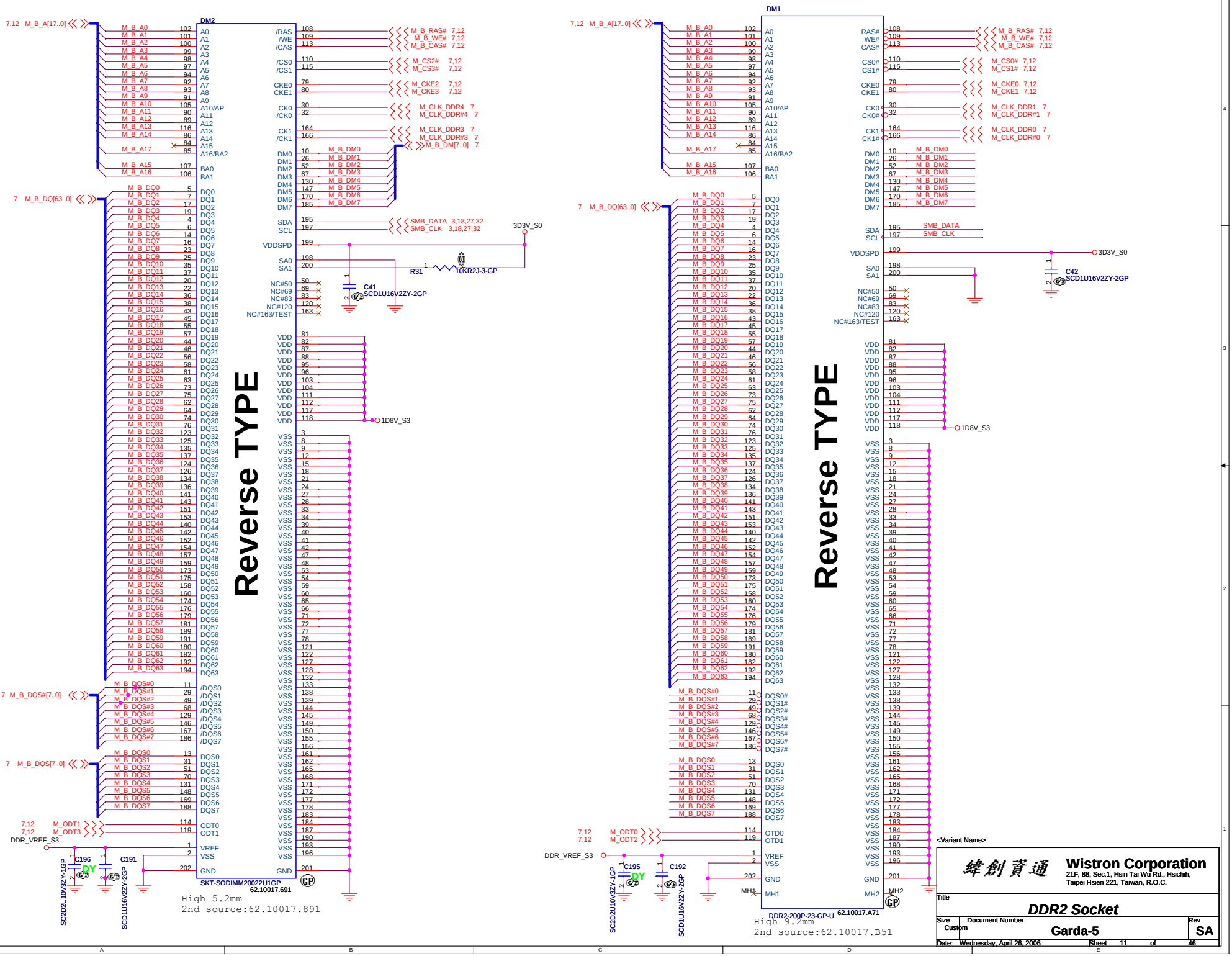
<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

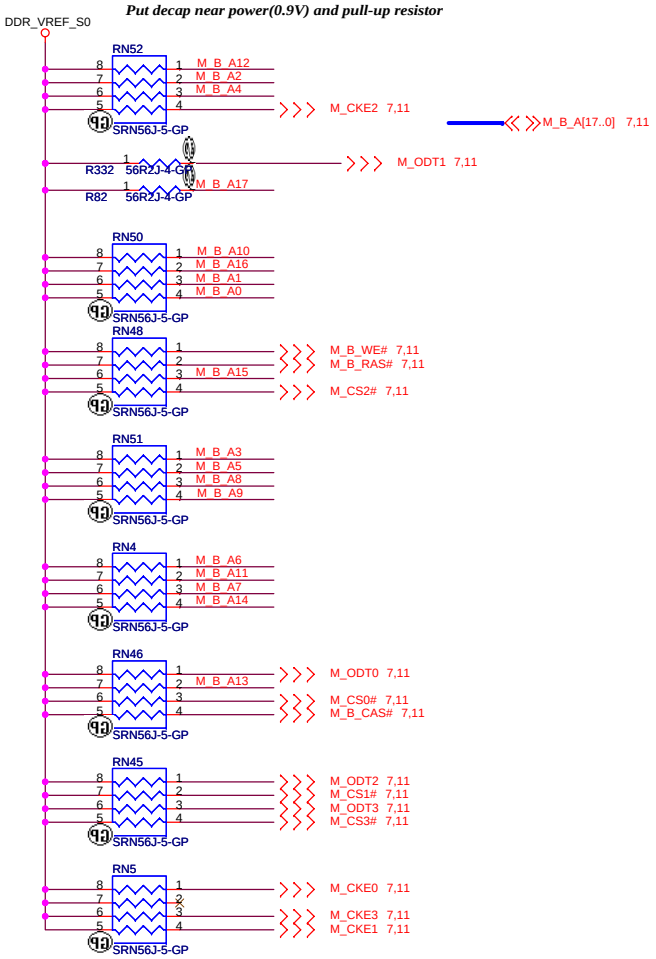
Title: RC410ME (5 of 5) Power

Size: A3 | Document Number: Garda-5 | Rev: SA

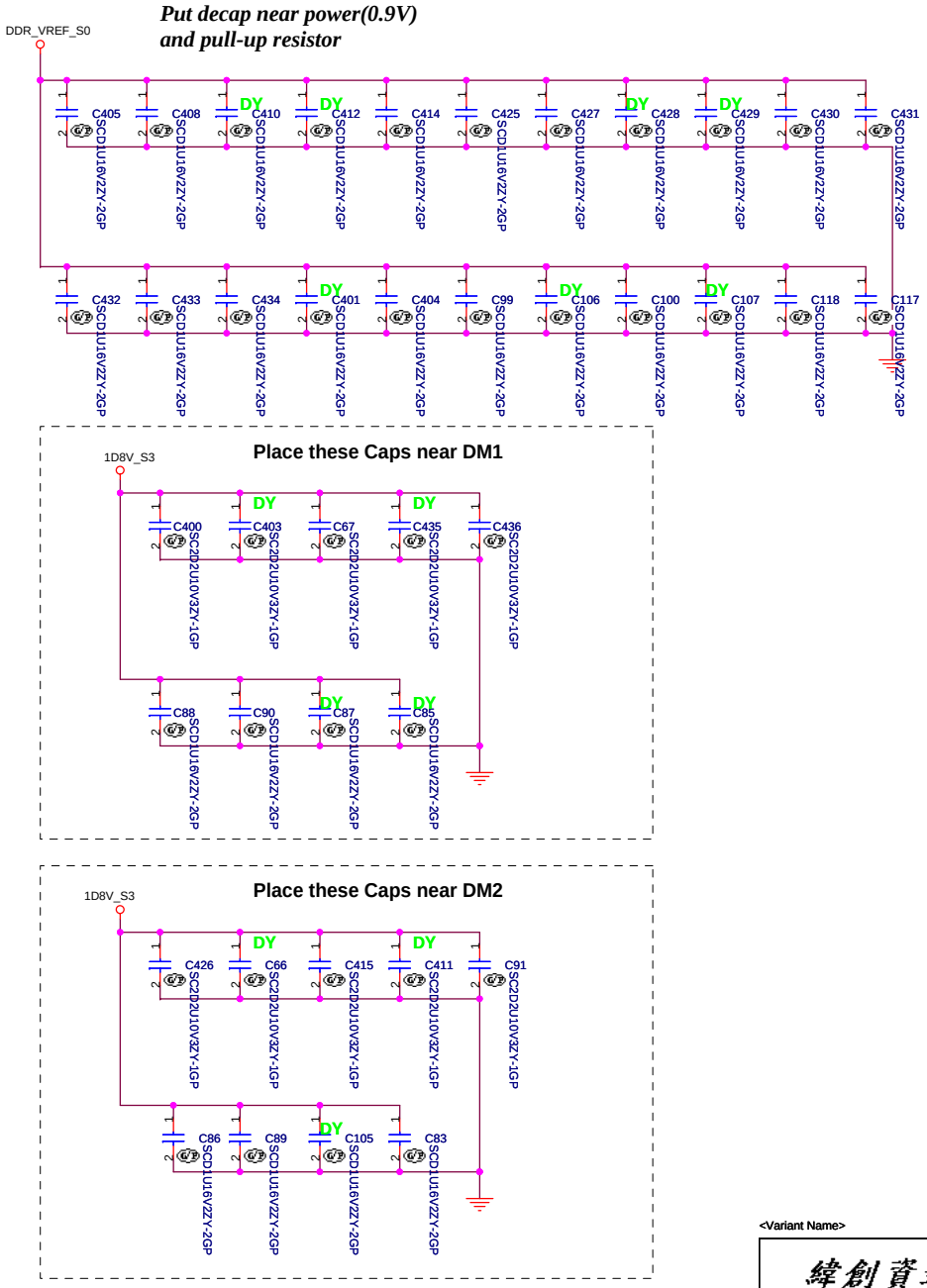
Date: Wednesday, April 26, 2006 | Sheet 10 of 46


DM2
Reverse TYPE
SKT-SODIMM20022U1GP
62.10017.691
High 5.2mm
2nd source:62.10017.891
DM1
Reverse TYPE
DDR2-200P-23-GP-U
62.10017.A71
High 9.2mm
2nd source:62.10017.B51
M_B_A[17..0]
M_B_DQ[63..0]
M_B_DQS#[7..0]
M_B_DQS[7..0]
M_B_DM[7..0]
M_B_RAS#
M_B_WE#
M_B_CAS#
M_CS2#
M_CS3#
M_CKE2
M_CKE3
M_CLK_DDR4
M_CLK_DDR#4
M_CLK_DDR3
M_CLK_DDR#3
M_CS0#
M_CS1#
M_CKE0
M_CKE1
M_CLK_DDR1
M_CLK_DDR#1
M_CLK_DDR0
M_CLK_DDR#0
M_ODT1
M_ODT3
M_ODT0
M_ODT2
SMB_DATA
SMB_CLK
3D3V_S0
1D8V_S3
DDR_VREF_S3
R31
10KR2J-3-GP
C41
C42
SCD1U16V2ZY-2GP
C196
C191
C195
C192
SC2D2U10V3ZY-1GP
DY
<Variant Name>
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
DDR2 Socket
Size
Custom
Document Number
Garda-5
Rev
SA
Date: Wednesday, April 26, 2006
Sheet 11 of 46

PARALLEL TERMINATION



Decoupling Capacitor



<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***DDR2 Termination Resistor***

Size	Document Number	Rev
A3	Garda-5	SA

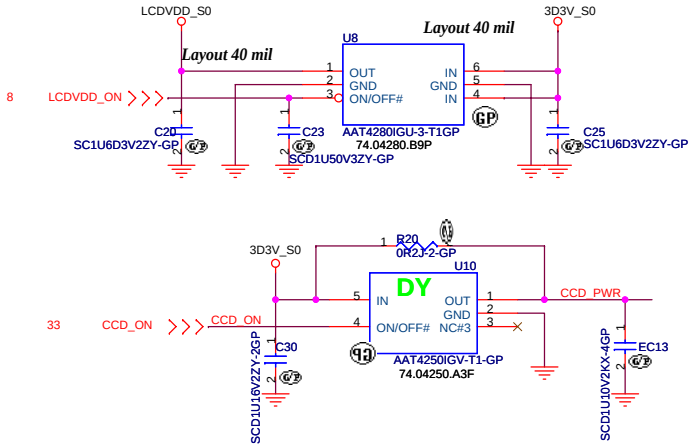
Date: Wednesday, April 26, 2006 Sheet 12 of 46

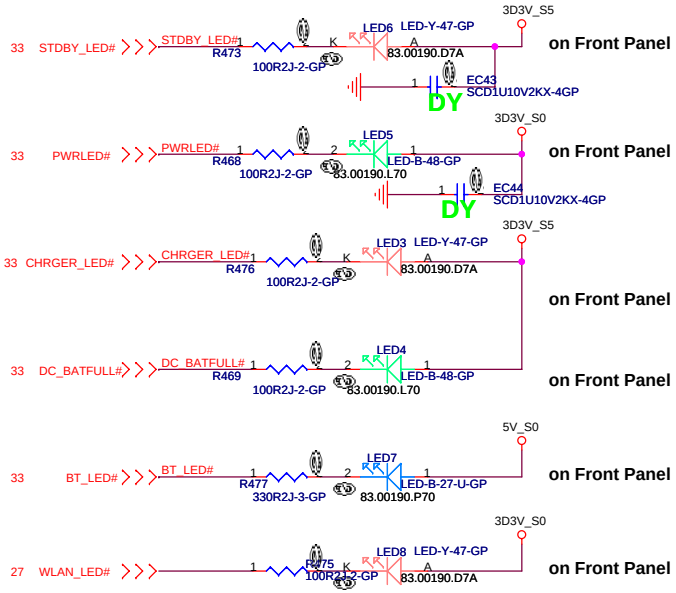
LCD/INVERTER/CCD CONN

CCD Pin	
Pin	Symbol
1	3.3V
2	USB-
3	USB+
4	GND
5	GND

Inverter Pin	
Pin	Symbol
1	Vin
2	Vin
3	PWM
4	BLON
5	GND
6	GND

Launch BD	
Pin	Symbol
1	3V_S0
2	PWRBTN#
3	PROGRAM#
4	EBUTTON#
5	INTERNET#
6	MAIL#
7	NC
8	MAIL_LED#
9	PWR_B_LED#
10	NC
11	INT_MICP
12	INT_MICN



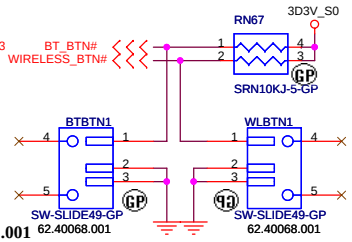


Charger:
OFF : Battery or DC only
Orange : Charging
Orange Blink : Battery low

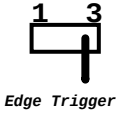
Power:
Green : S0
Orange : S3
Orange Blinking : Enter S4

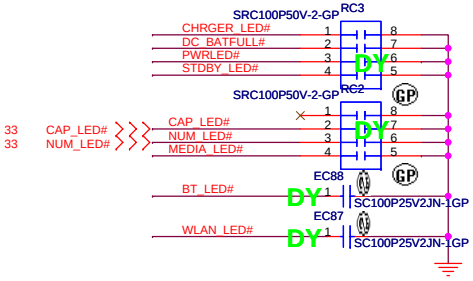
Front panel

LED	V	V	V	V
Button	V	V		
	BlutTooth	Wireless	Charger	Power2

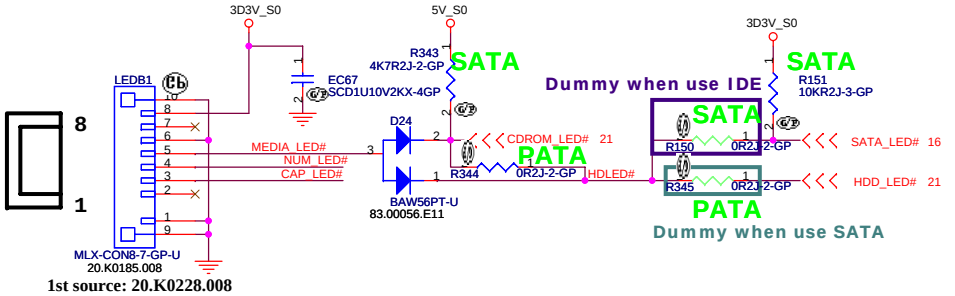


2nd source: 62.40066.001

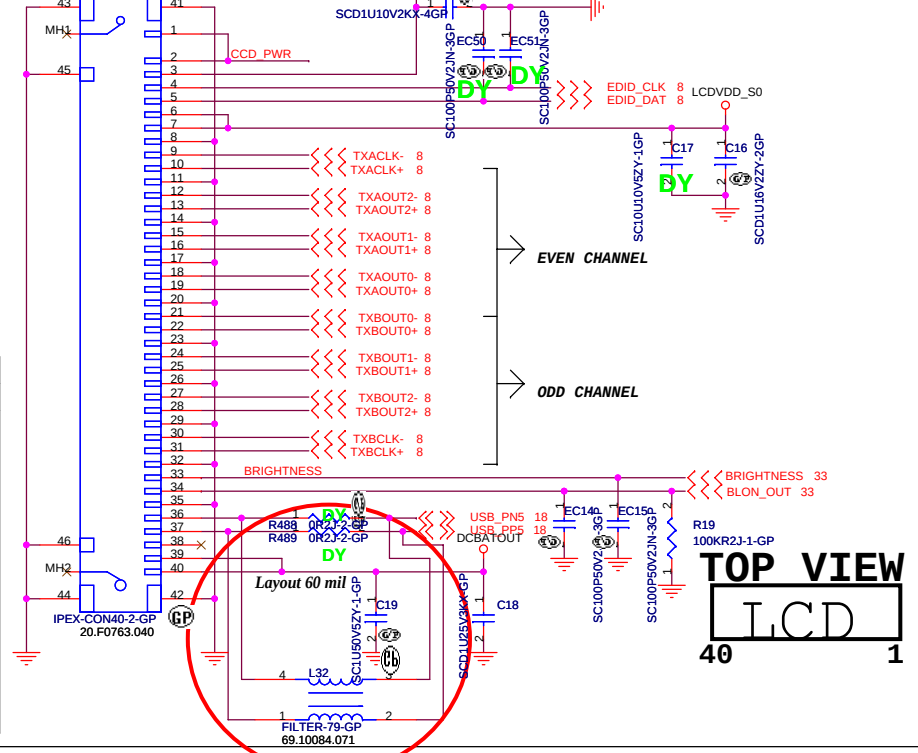




LED BD CONN



1st source: 20.K0228.008



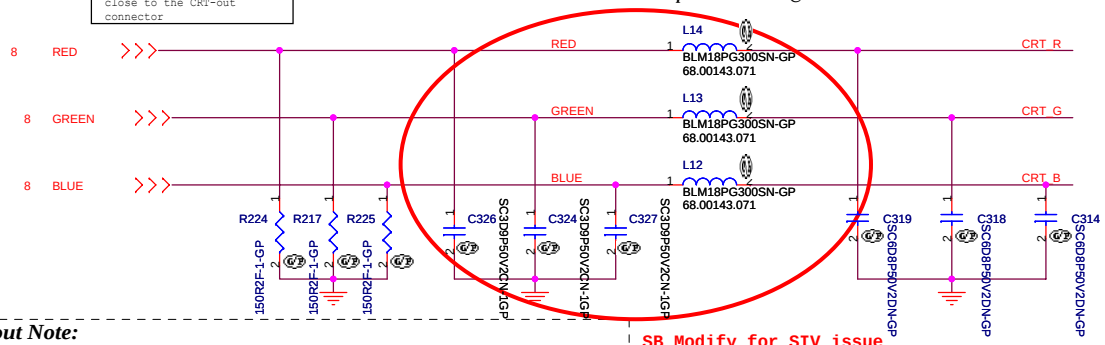
<Variant Name>

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	LCD / LAUNCH / LEDs
Size A3	Document Number: Gards-5
Rev	-1
Date: Wednesday, April 26, 2006	Sheet 13 of 46

CRT I/F & CONNECTOR

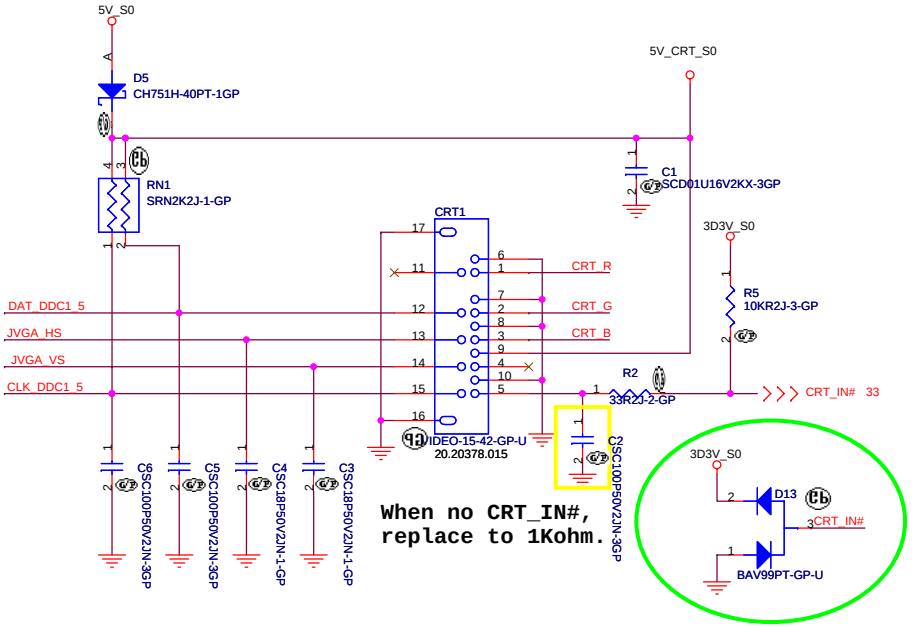
Layout Note:
Place these resistors close to the CRT-out connector

Ferrite bead impedance: 30 ohm@100MHz

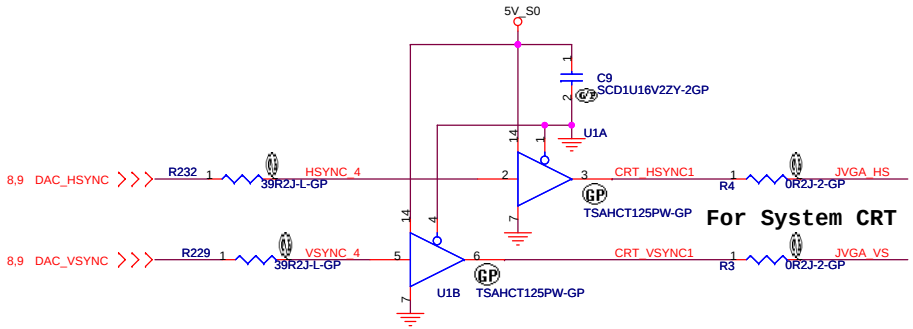


SB Modify for SIV issue

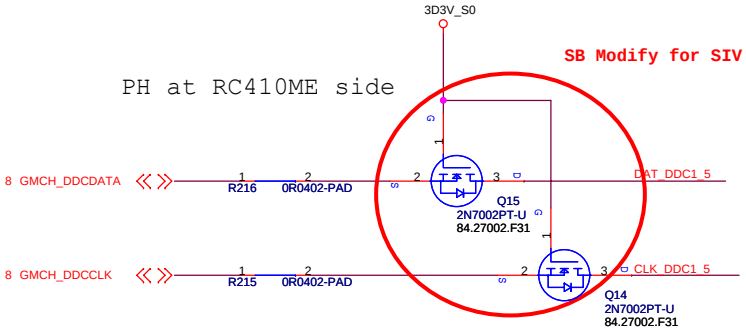
Layout Note:
**** Must be a ground return path between this ground and the ground on the VGA connector.***
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.



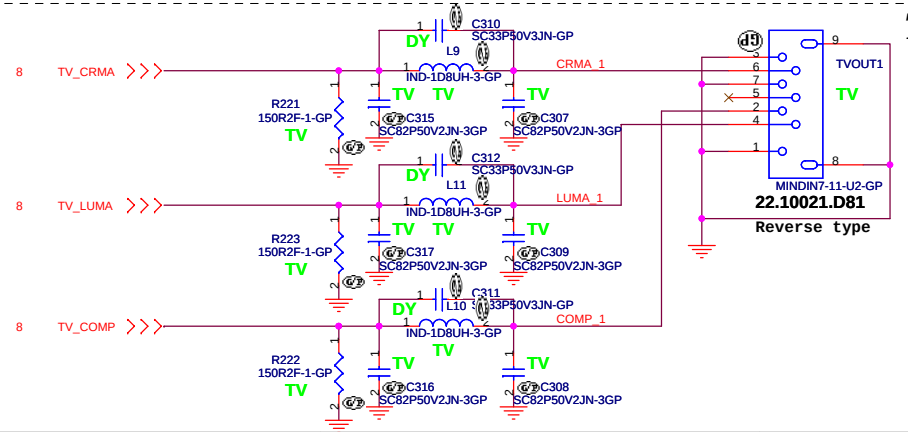
Hsync & Vsync level shift

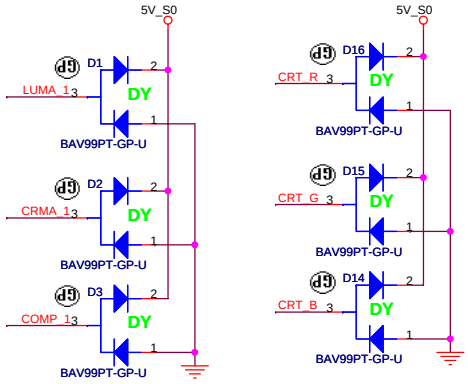


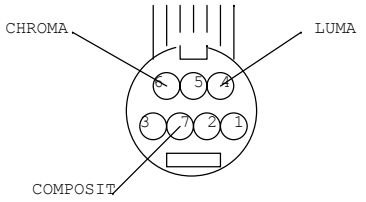
DDC_CLK & DATA level shift



TV OUT CONN







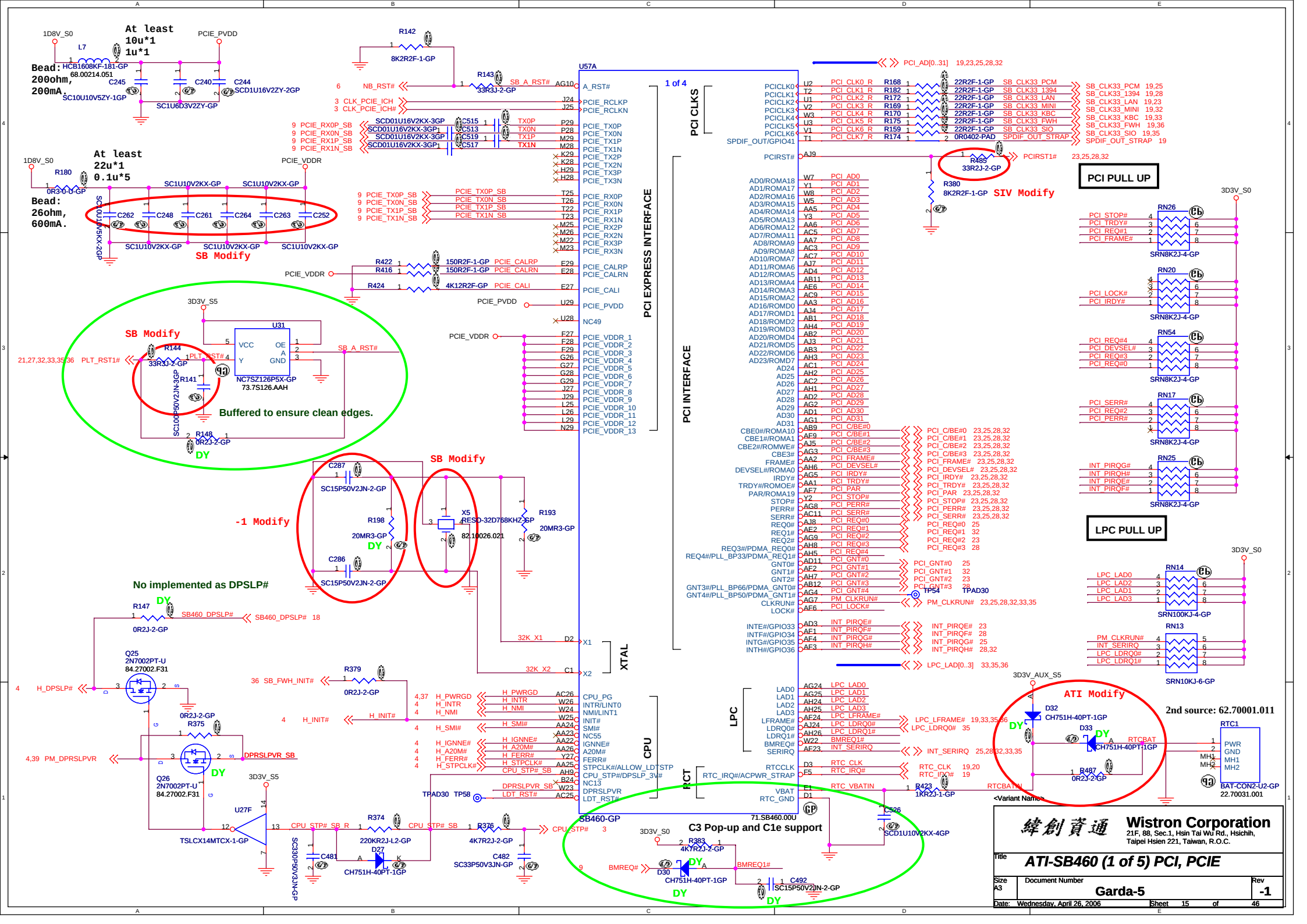
<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

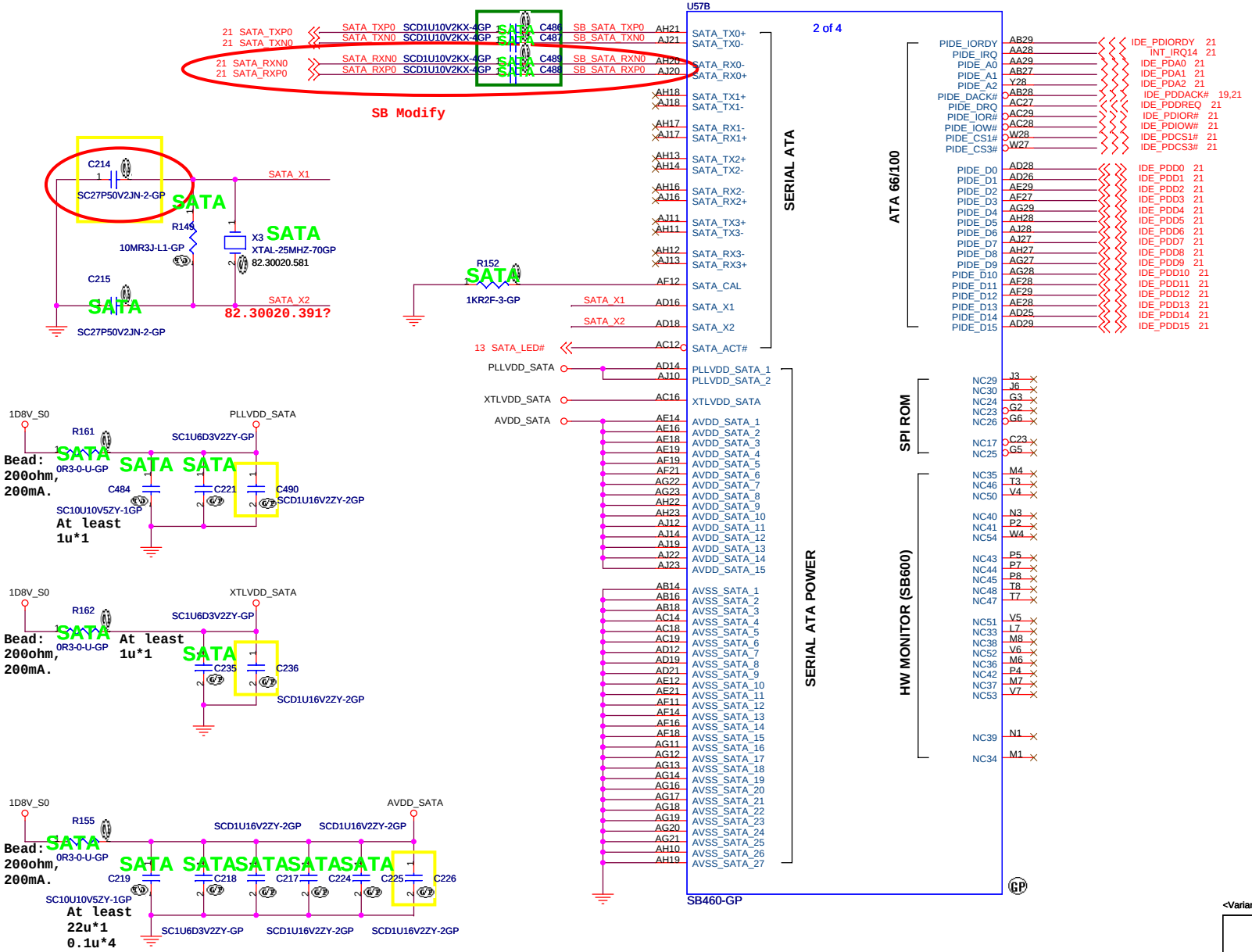
Title: **CRT/TV Connector**

Size	Document Number	Rev
A3	Garda-5	SB

Date: Wednesday, April 26, 2006 Sheet 14 of 46


U57A
1 of 4
SB460-GP
71.SB460.00U
PCI CLKS
PCI EXPRESS INTERFACE
PCI INTERFACE
XTAL
CPU
LPC
RCT
PCI PULL UP
LPC PULL UP
SB Modify
SIV Modify
ATI Modify
-1 Modify
DY
Buffered to ensure clean edges.
No implemented as DPSLP#
C3 Pop-up and C1e support
2nd source: 62.70001.011
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
ATI-SB460 (1 of 5) PCI, PCIE
Garda-5
-1
Wednesday, April 26, 2006
Sheet 15 of 46

When no SATA replace to 0 ohm.



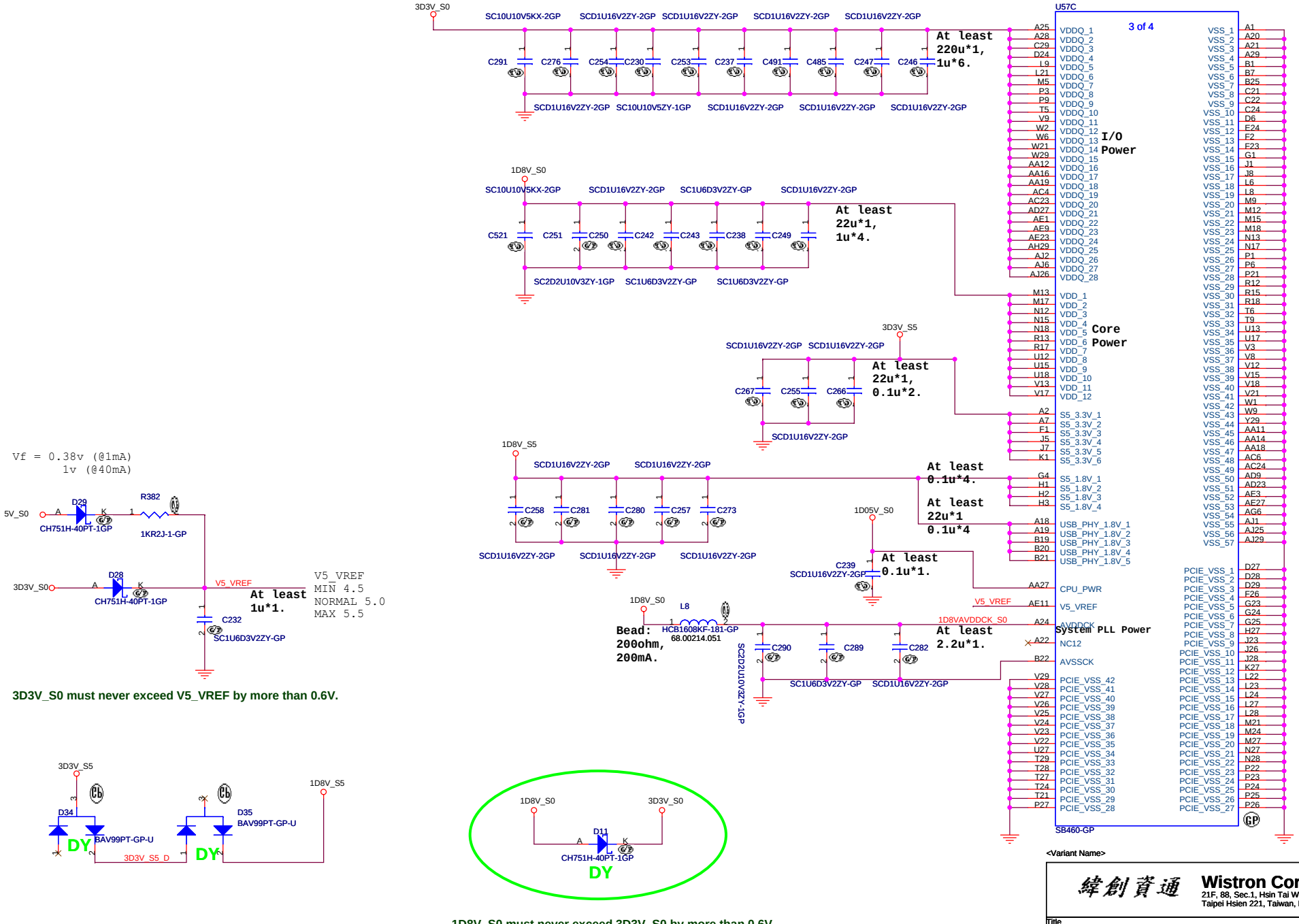
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

<Variant Name>

Title: ATI-SB460 (2 of 5) IDE/SATA

Size: A3 | Document Number: Garda-5 | Rev: SB

Date: Wednesday, April 26, 2006 | Sheet 16 of 46



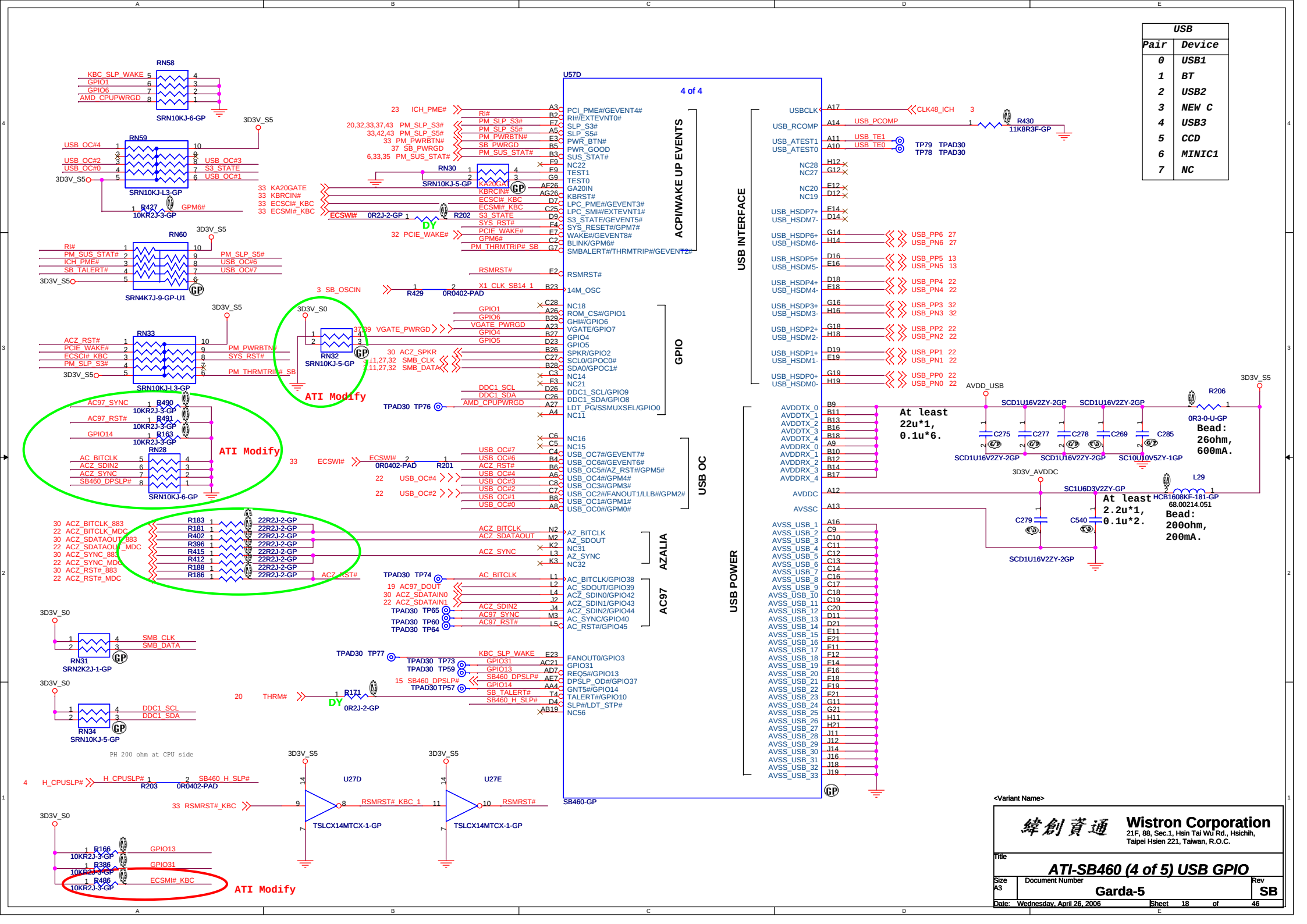
<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

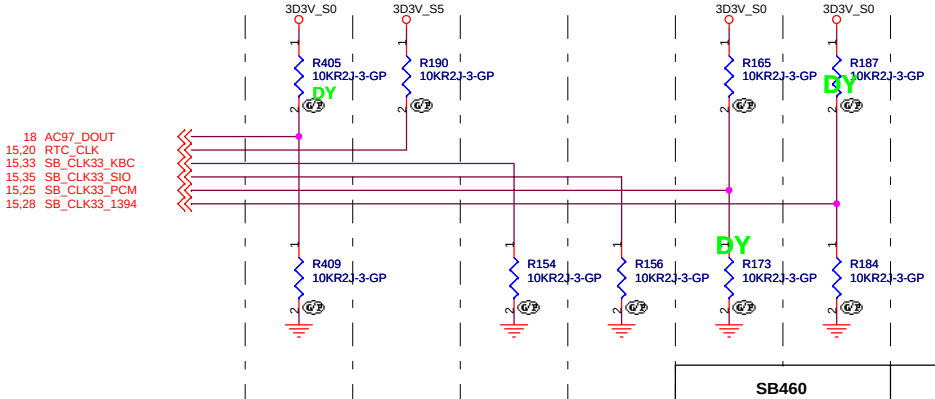
Title: **ATI-SB460 (3 of 5) POWER**

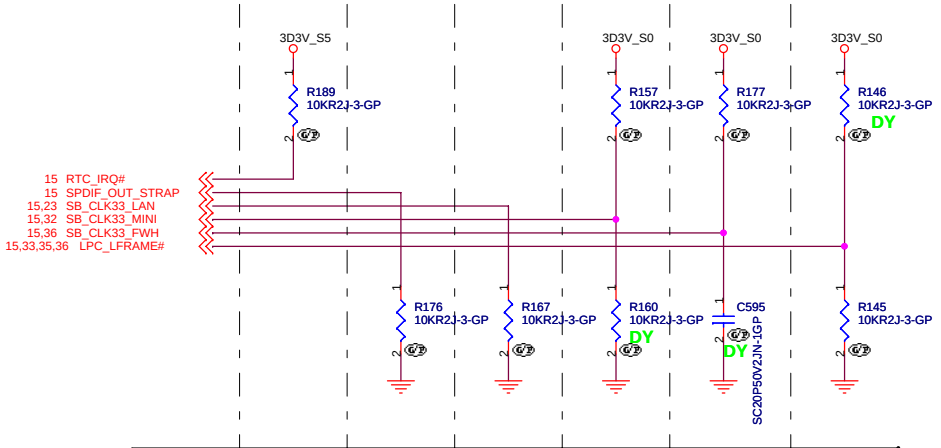
Size	Document Number	Rev
A3	Garda-5	SA

Date: Wednesday, April 26, 2006 Sheet 17 of 46


USB
Pair Device
0 USB1
1 BT
2 USB2
3 NEW C
4 USB3
5 CCD
6 MINIC1
7 NC
U57D
4 of 4
SB460-GP
ACPI/WAKE UP EVENTS
GPIO
USB OC
AZALIA
AC97
USB INTERFACE
USB POWER
ATI Modify
ATI Modify
ATI Modify
At least 22u*1, 0.1u*6.
At least 2.2u*1, 0.1u*2.
Bead: 26ohm, 600mA.
Bead: 200ohm, 200mA.
PH 200 ohm at CPU side
<Variant Name>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ATI-SB460 (4 of 5) USB GPIO
Size A3
Document Number Garda-5
Rev SB
Date: Wednesday, April 26, 2006
Sheet 18 of 46

REQUIRED STRAPS





PCI_CLK0 PCM
PCI_CLK1 IEEE1394
PCI_CLK2 LAN
PCI_CLK3 MINI
PCI_CLK4 KBC
PCI_CLK5 FWH
PCI_CLK6 SIO
PCI_CLK7 SPDIFOUT

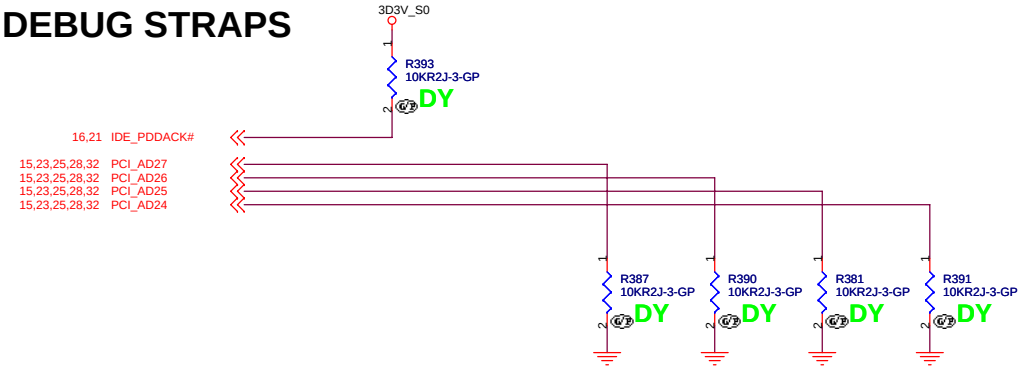
	AC_SDOUT	RTC_CLK	PCI_CLK4	PCI_CLK6	SB460 PCI_CLK0	SB460 PCI_CLK1	SB600 PCI_CLK0	SB600 PCI_CLK1
PULL HIGH	USE DEBUG STRAPS	INTERNAL RTC DEFAULT	USE INT. USB PLL48	CPU IF=K8	ROM TYPE: H, H = PCI ROM; H, L = LPC I ROM DEFAULT; L, H = LPC II ROM; L, L = FWH ROM		ROM TYPE: H, H = PCI ROM; H, L = SPI ROM; L, H = LPC ROM DEFAULT; L, L = FWH ROM	
PULL LOW	DISABLE DEBUG STRAPS DEFAULT	EXTERNAL RTC	USE EXT. USB 48MHZ SOURCE DEFAULT	CPU IF=P4 DEFAULT	NOTE: FOR SB460, PCICLK[8:7] ARE CONNECTED TO SUBSTRATE BALLS PCICLK[1:0]			

Require upper 12 addr bits set to "1".

	ACPWRON	SPDIF_OUT	PCI_CLK2	PCI_CLK3	PCI_CLK5	LFRAME#
PULL HIGH	MANUAL PWR ON DEFAULT	SIO 24MHz	48M XTAL MODE NOT SUPPORTED	USB PHY POWERDOWN DISABLE DEFAULT	PCIE LANE AUTO DETECT DEFAULT	ENABLE THERMTRIP# DEFAULT
PULL LOW	AUTO PWR ON	SIO 48MHz DEFAULT	48MHZ OSC MODE DEFAULT	USB PHY POWERDOWN ENABLE	PCIE LANE FORCING TO 2 LANES DEBUG ONLY	DISABLE THERMTRIP#

USB wake from S5 supported.

DEBUG STRAPS



	IDE_DACK#	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET DEFAULT		BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	
PULL LOW	USE SHORT RESET		USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	NOTE: FOR SB460, PCI_AD23 IS RESERVED

SB460 ONLY SB600 ONLY SB600 ONLY

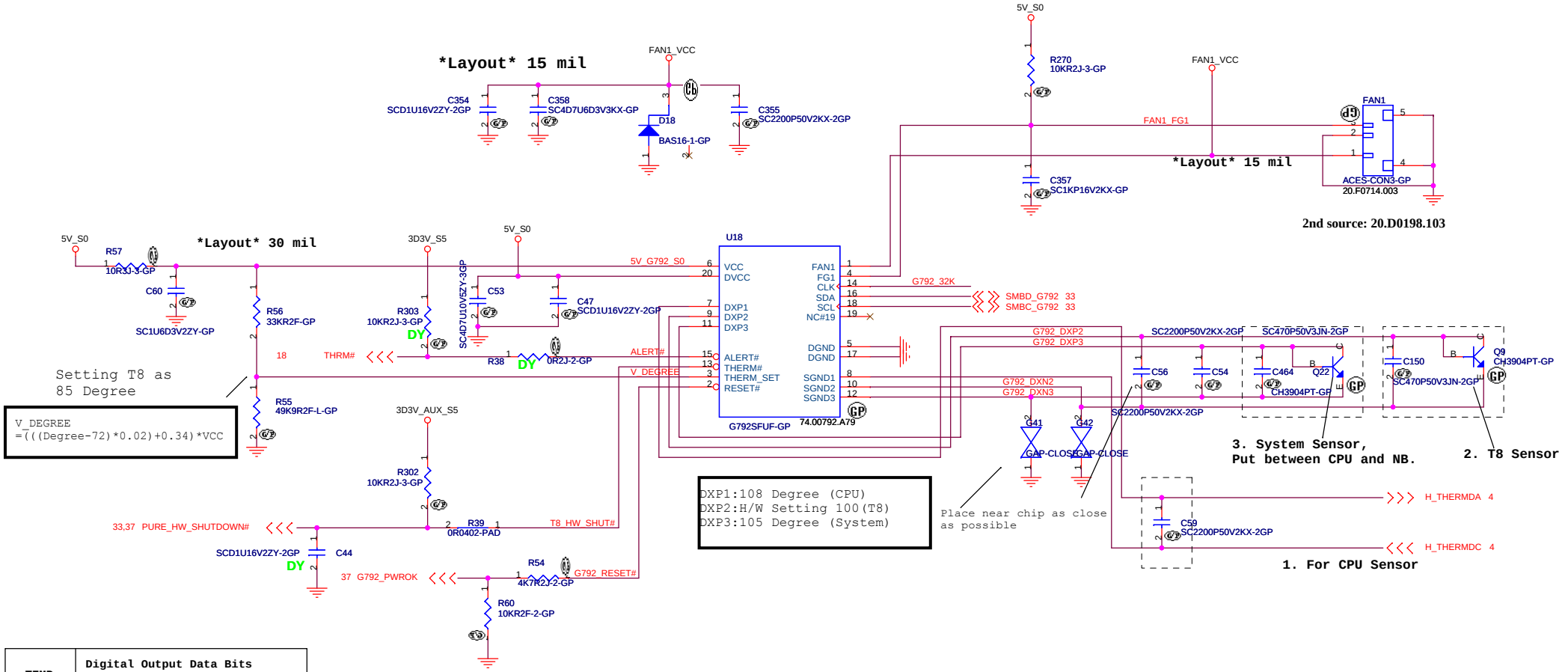
<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

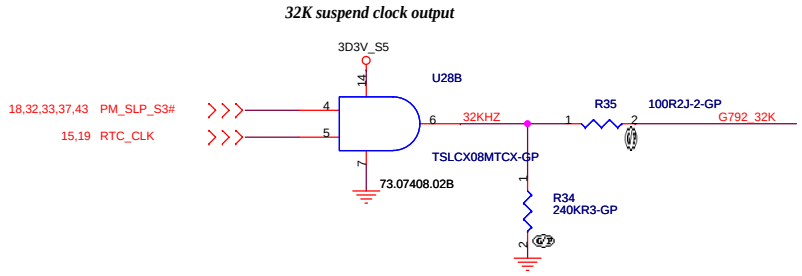
Title: ATI-SB460 (5 of 5) STRAPPING

Size: A3 | Document Number: Garda5 | Rev: SA

Date: Wednesday, April 26, 2006 | Sheet 19 of 46



TEMP.	Digital Output Data Bits			
	Sign	MSB	LSB	EXT
+127.875	0	111	1111	111
+126.375	0	111	1110	011
+25.5	0	001	1001	100
+1.75	0	000	0001	110
+0.5	0	000	0000	100
+0.125	0	000	0000	001
-0.125	1	111	1111	111
-1.125	1	111	1110	111
-25.5	1	110	0110	100
-55.25	1	100	1000	110
-65.000	1	011	1111	000



<Variant Name>

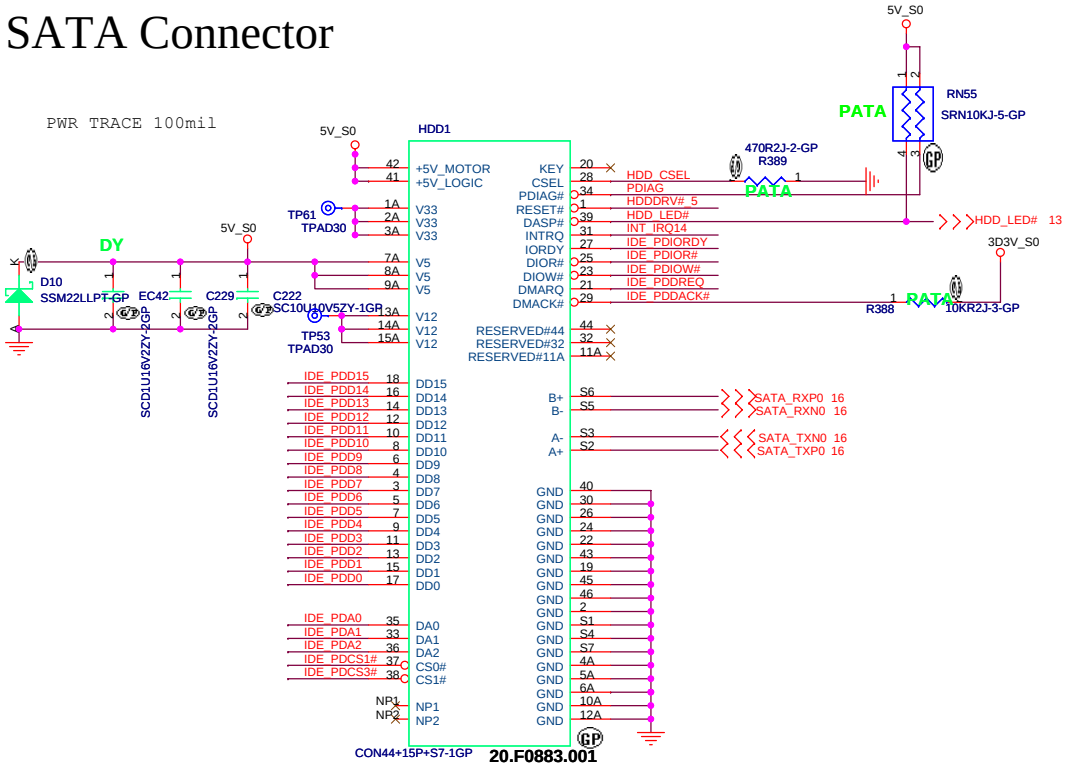
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Thermal/Fan Controllor G792***

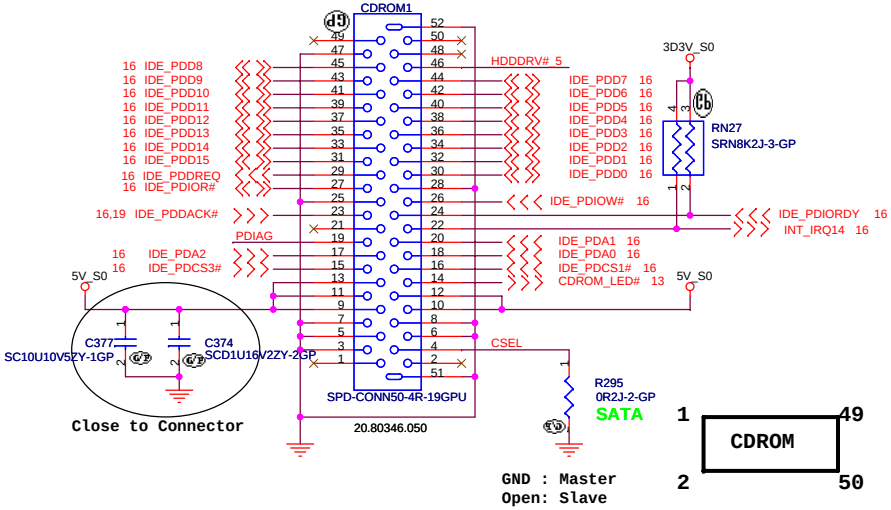
Size	Document Number	Rev
Custom	Garda-5	SA

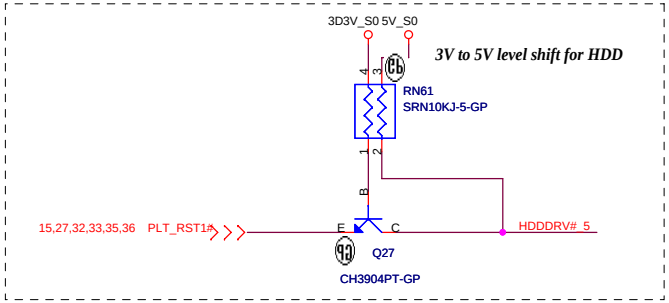
Date: Wednesday, April 26, 2006 Sheet 20 of 46

SATA Connector



CDROM Connector





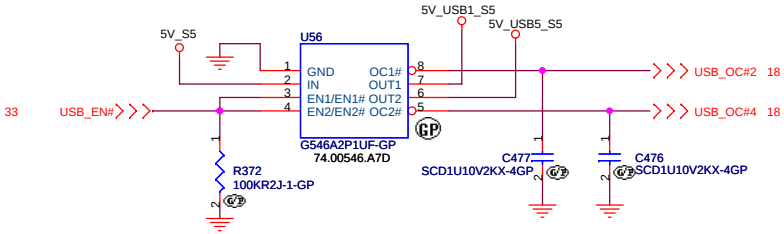
<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

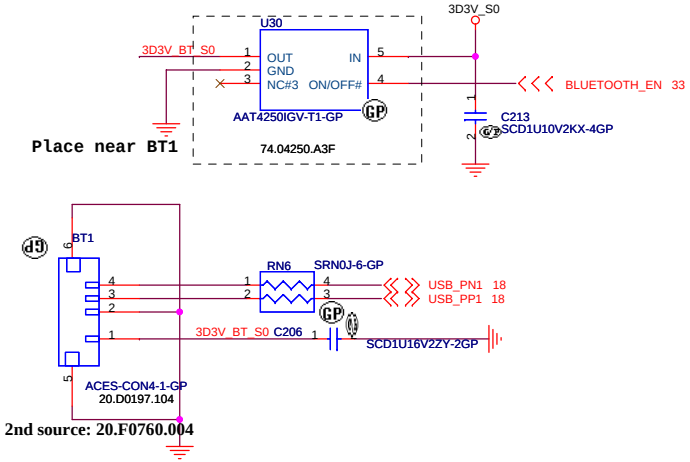
Title: **SATA/PATA HDD / ODD**

Size	Document Number	Rev
A3	Garda-5	SA

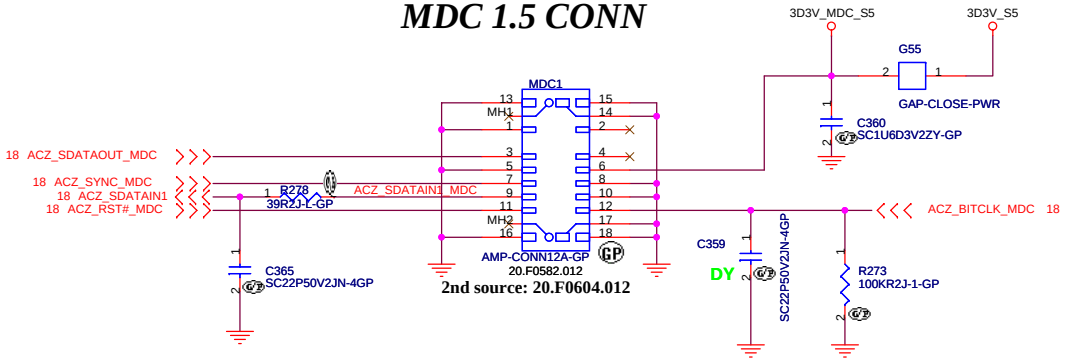
Date: Wednesday, April 26, 2006 Sheet 21 of 46



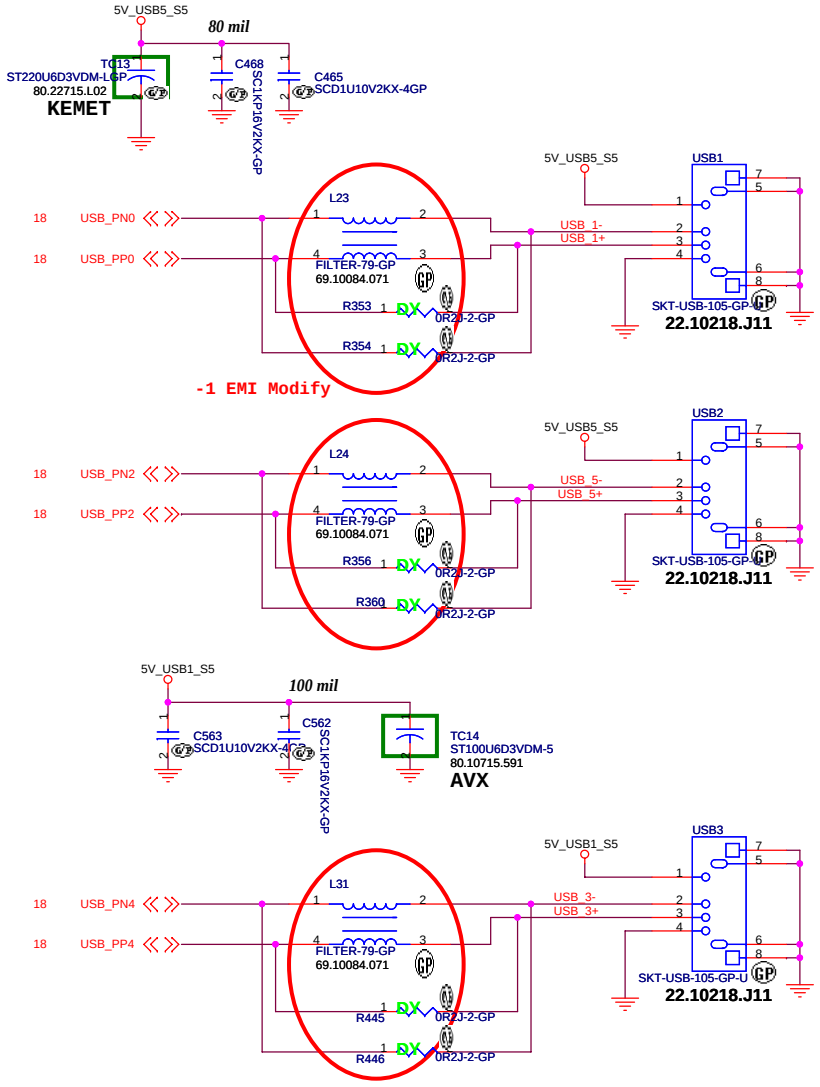
BLUETOOTH MODULE CONNECTOR



MDC 1.5 CONN



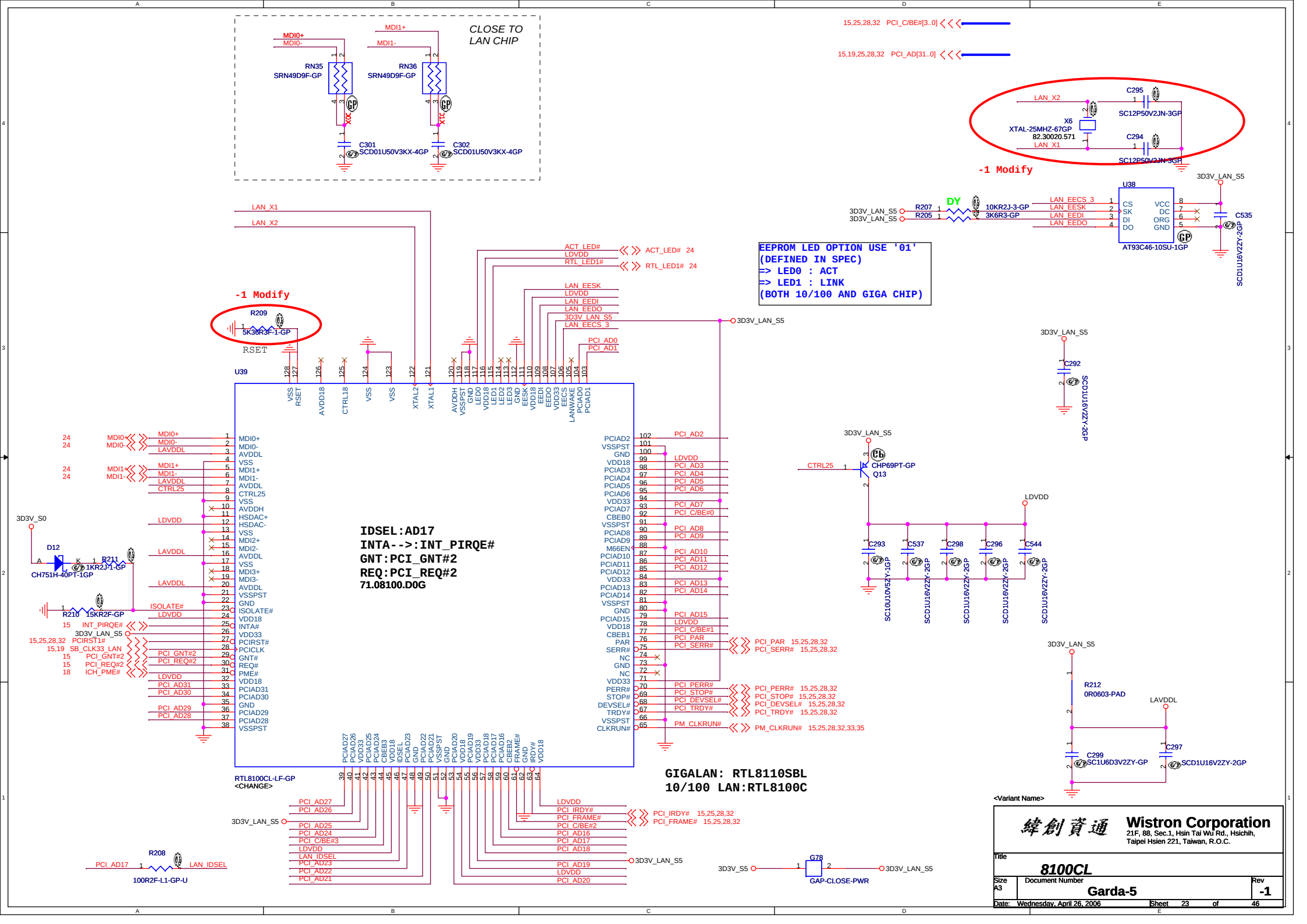
USB PORT



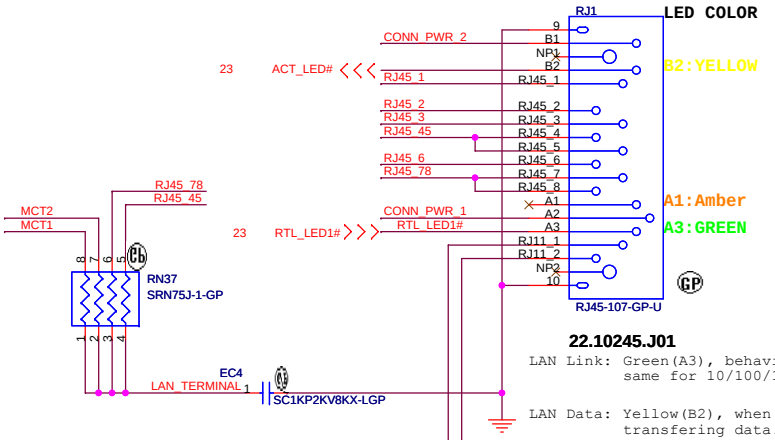
<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **USB and MDC I/F**		
Size: A3	Document Number: **Garda-5**	Rev: **-1**
Date: Wednesday, April 26, 2006	Sheet 22 of 46	


CLOSE TO LAN CHIP
MDI0+
MDI0-
MDI1+
MDI1-
RN35 SRN49D9F-GP
RN36 SRN49D9F-GP
C301 SCD01U50V3KX-4GP
C302 SCD01U50V3KX-4GP
15,25,28,32 PCI_C/BE#[3..0]
15,19,25,28,32 PCI_AD[31..0]
LAN_X2
LAN_X1
X6 XTAL-25MHZ-67GP 82.30020.571
C295 SC12P50V2JN-3GP
C294 SC12P50V2JN-3GP
-1 Modify
U38 AT93C46-10SU-1GP
3D3V_LAN_S5
R207 DY
R205
10KR2J-3-GP
3K6R3-GP
LAN_EECS_3
LAN_EESK
LAN_EEDI
LAN_EEDO
C535 SCD1U16V2ZY-2GP
EEPROM LED OPTION USE '01'
(DEFINED IN SPEC)
=> LED0 : ACT
=> LED1 : LINK
(BOTH 10/100 AND GIGA CHIP)
ACT_LED# 24
RTL_LED1# 24
-1 Modify
R209 5K36R3F-1-GP
RSET
U39
IDSEL:AD17
INTA-->:INT_PIRQE#
GNT:PCI_GNT#2
REQ:PCI_REQ#2
71.08100.D0G
RTL8100CL-LF-GP
<CHANGE>
GIGALAN: RTL8110SBL
10/100 LAN:RTL8100C
C292 SCD1U16V2ZY-2GP
CHP69PT-GP Q13
CTRL25
LDVDD
C293 SC10U10V5ZY-1GP
C537 C298 C296 C544 SCD1U16V2ZY-2GP
D12 CH751H-40PT-1GP
R211 1KR2J-1-GP
R210 15KR2F-GP
ISOLATE#
INT_PIRQE#
PCIRST1#
SB_CLK33_LAN
PCI_GNT#2
PCI_REQ#2
ICH_PME#
R212 0R0603-PAD
C299 SC1U6D3V2ZY-GP
C297 SCD1U16V2ZY-2GP
R208 100R2F-L1-GP-U
PCI_AD17
LAN_IDSEL
G78 GAP-CLOSE-PWR
3D3V_S5
<Variant Name>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title 8100CL
Size A3
Document Number Garda-5
Rev -1
Date: Wednesday, April 26, 2006
Sheet 23 of 46

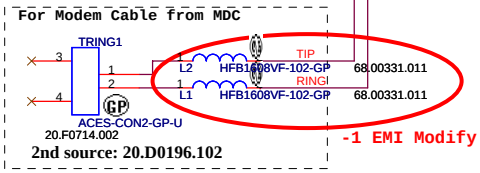
LAN Connector

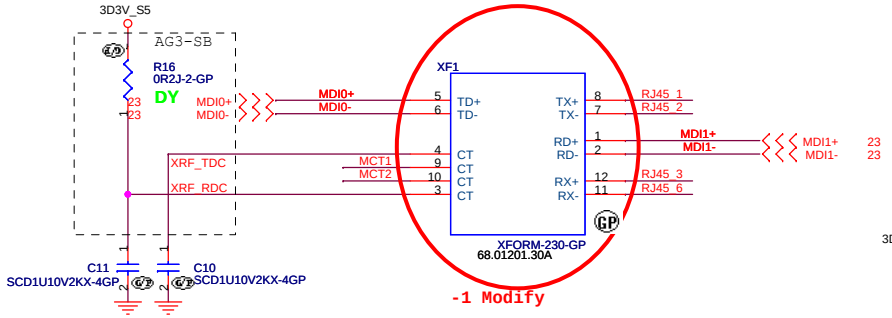


22.10245.J01

LAN Link: Green(A3), behavior is the same for 10/100/1000 bits

LAN Data: Yellow(B2), when LAN is transfering data.



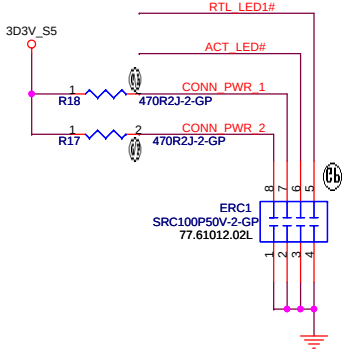


1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except RJ-45 moat.

RJ11 signal must leave the other signal or power plane 100mil.

DOC_TIP,DOC_RING,TIP,RING:
W/S : 10/100 @ Surface layers
10/20 @ Inner layers

10/100 LAN Transformer	RJ45 PIN
TD+ --> TX+	RJ45-1
TD- --> TX-	RJ45-2
RD+ --> RX+	RJ45-3
RD- --> RX-	RJ45-6



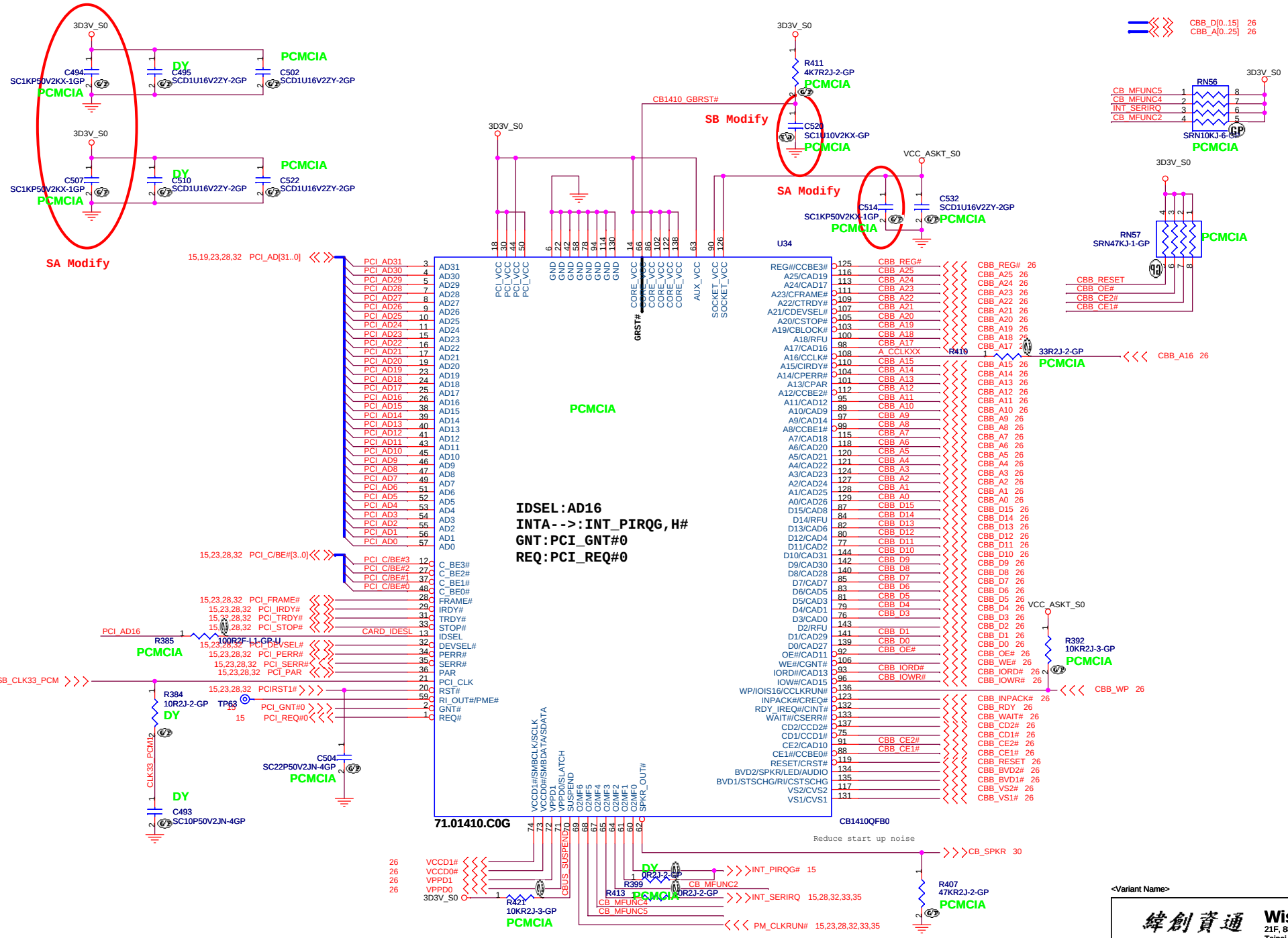
<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **LAN Connector**

Size	Document Number	Rev
A3	Garda-5	-1

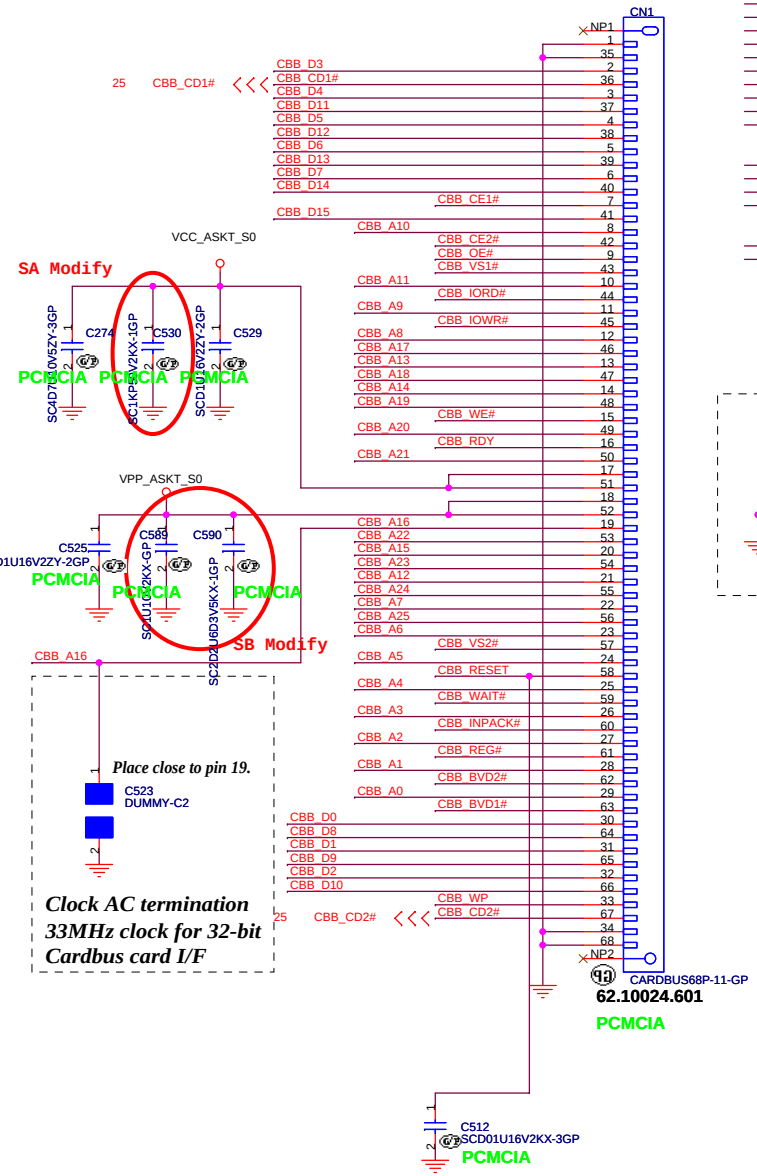
Date: Wednesday, April 26, 2006 Sheet 24 of 46



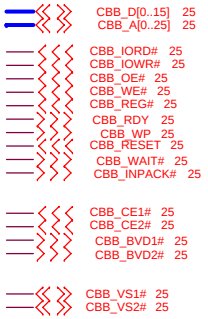
<variant_name>

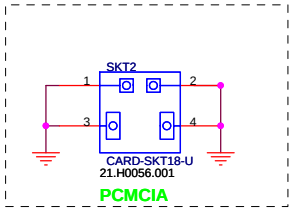
緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***CardBus_ENE CB1410***	
Size A3	Document Number **Garda-5**	Rev **SA**
Date: Wednesday, April 26, 2006	Sheet 25 of 46	

PCMCIA Socket

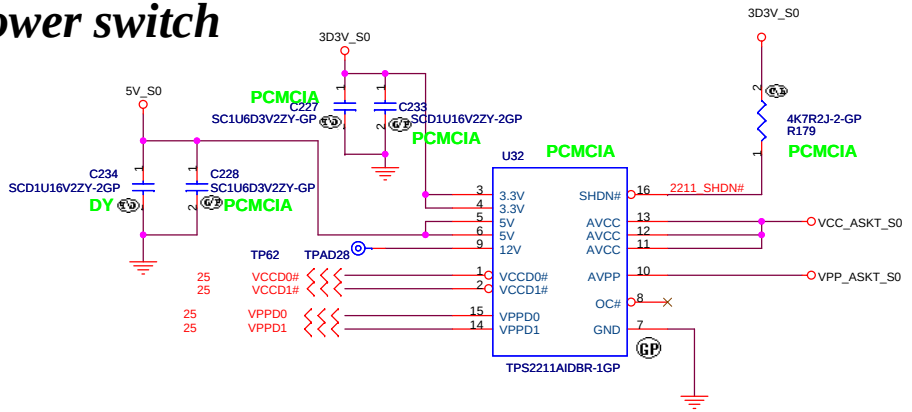


Cardbus I/F





Power switch

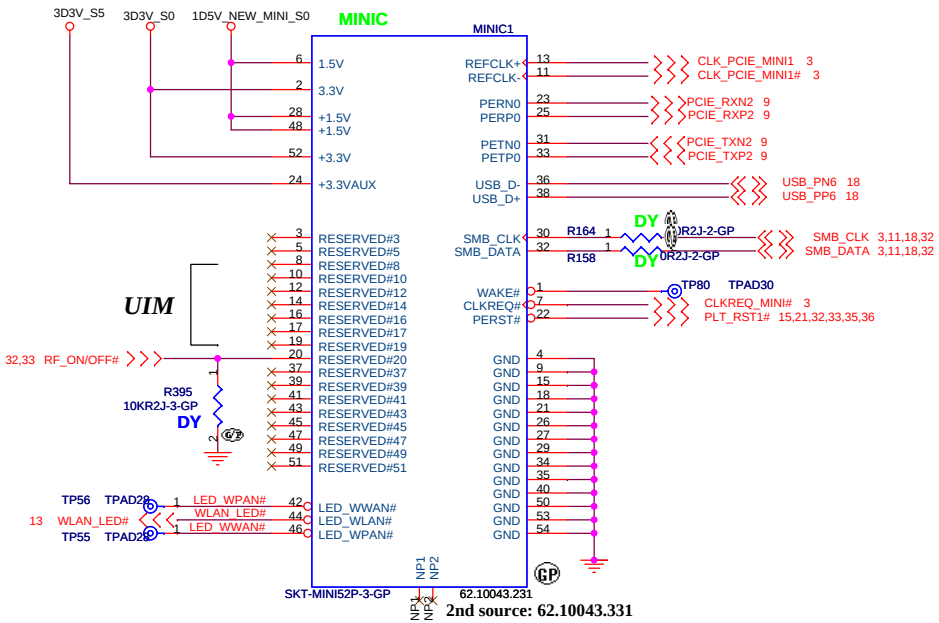


<Variant Name>

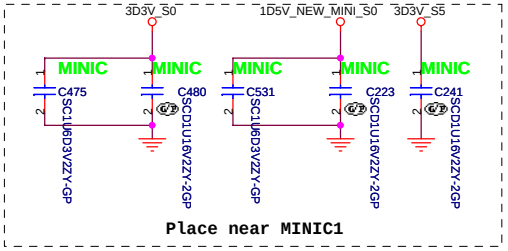
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

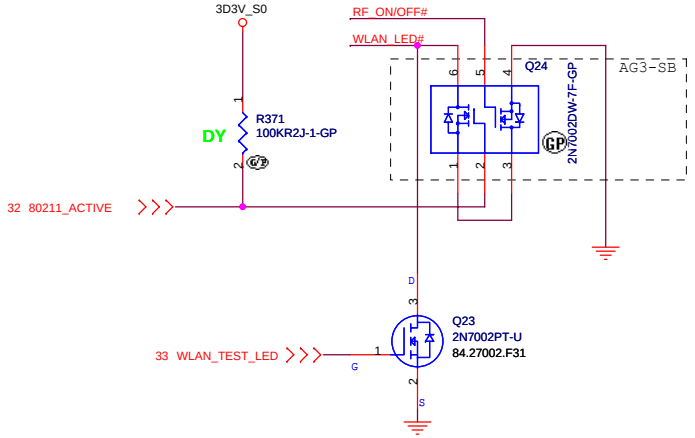
Title: PCMCIA		
Size: A3	Document Number: Garda-5	Rev: SB
Date: Wednesday, April 26, 2006	Sheet 26 of 46	

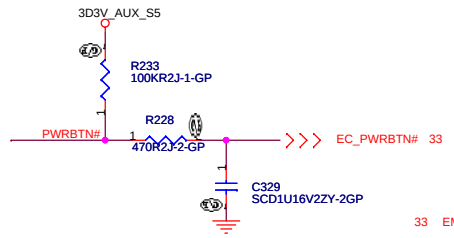
Mini Card Connector

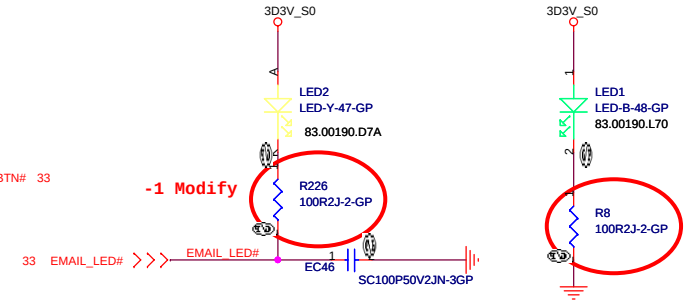


2nd source: 62.10043.331

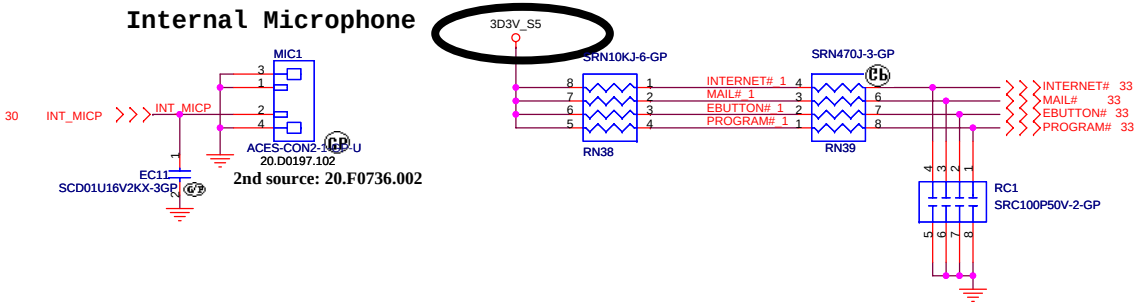








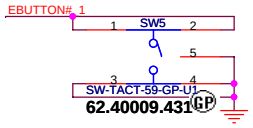
Internal Microphone



2nd source: 20.F0736.002

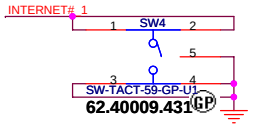
E-Button

TOP VIEW RIGHT 4



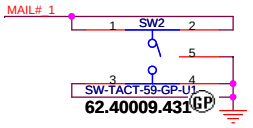
Internet Button

TOP VIEW RIGHT 3



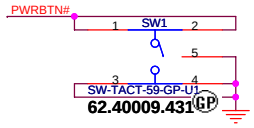
Mail Button

TOP VIEW RIGHT 2



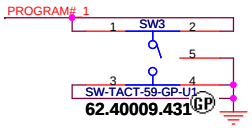
Power Button

TOP VIEW RIGHT 1



Program Button

TOP VIEW RIGHT 5



LED				V	V
Button	V	V	V	V	V
	Program Button	E-Button	Internet Button	Mail Button	Power Button

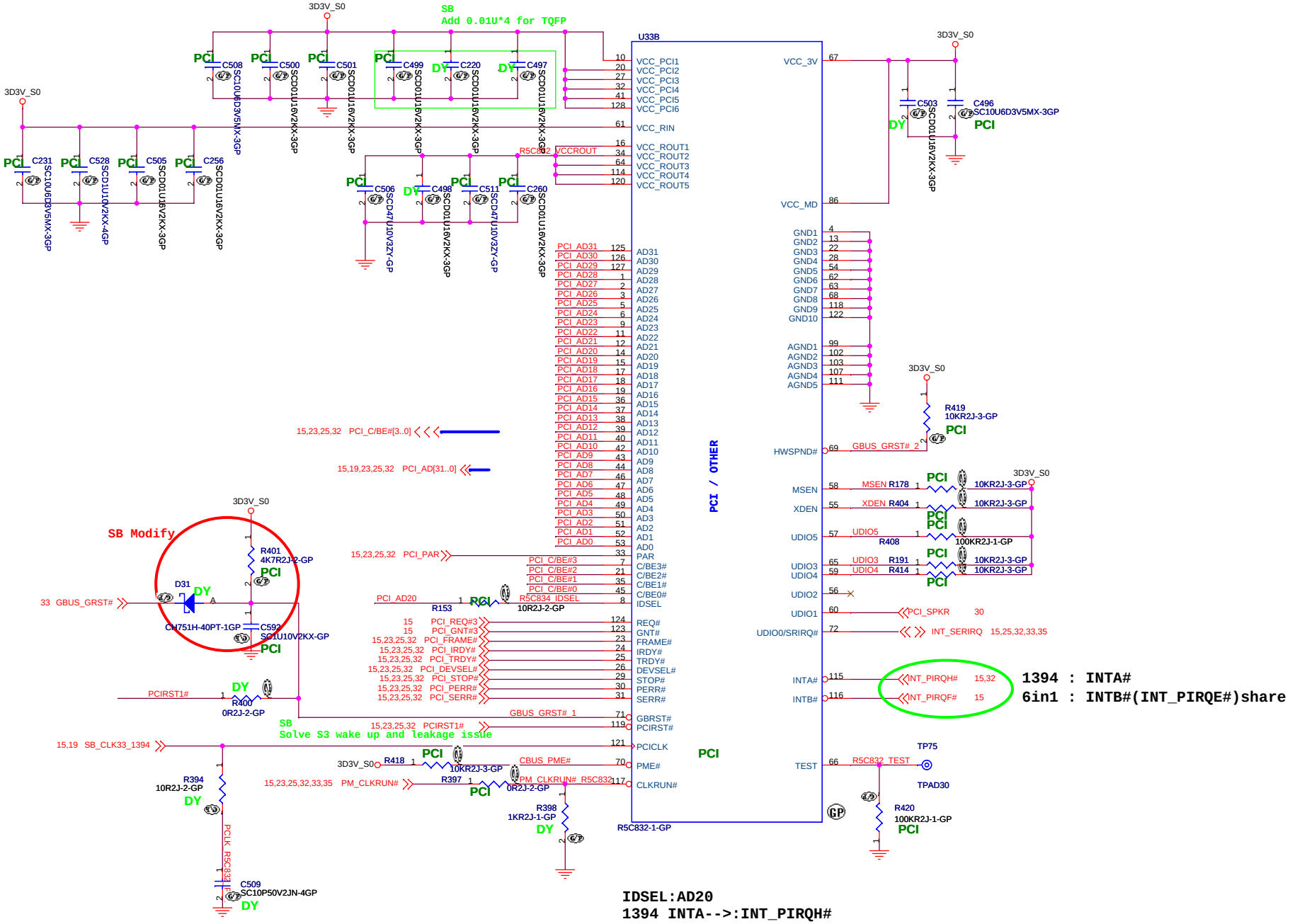
<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***MINI CARD / Launch Button***

Size	Document Number	Rev
A3	Garda-5	-1

Date: Wednesday, April 26, 2006 Sheet 27 of 46



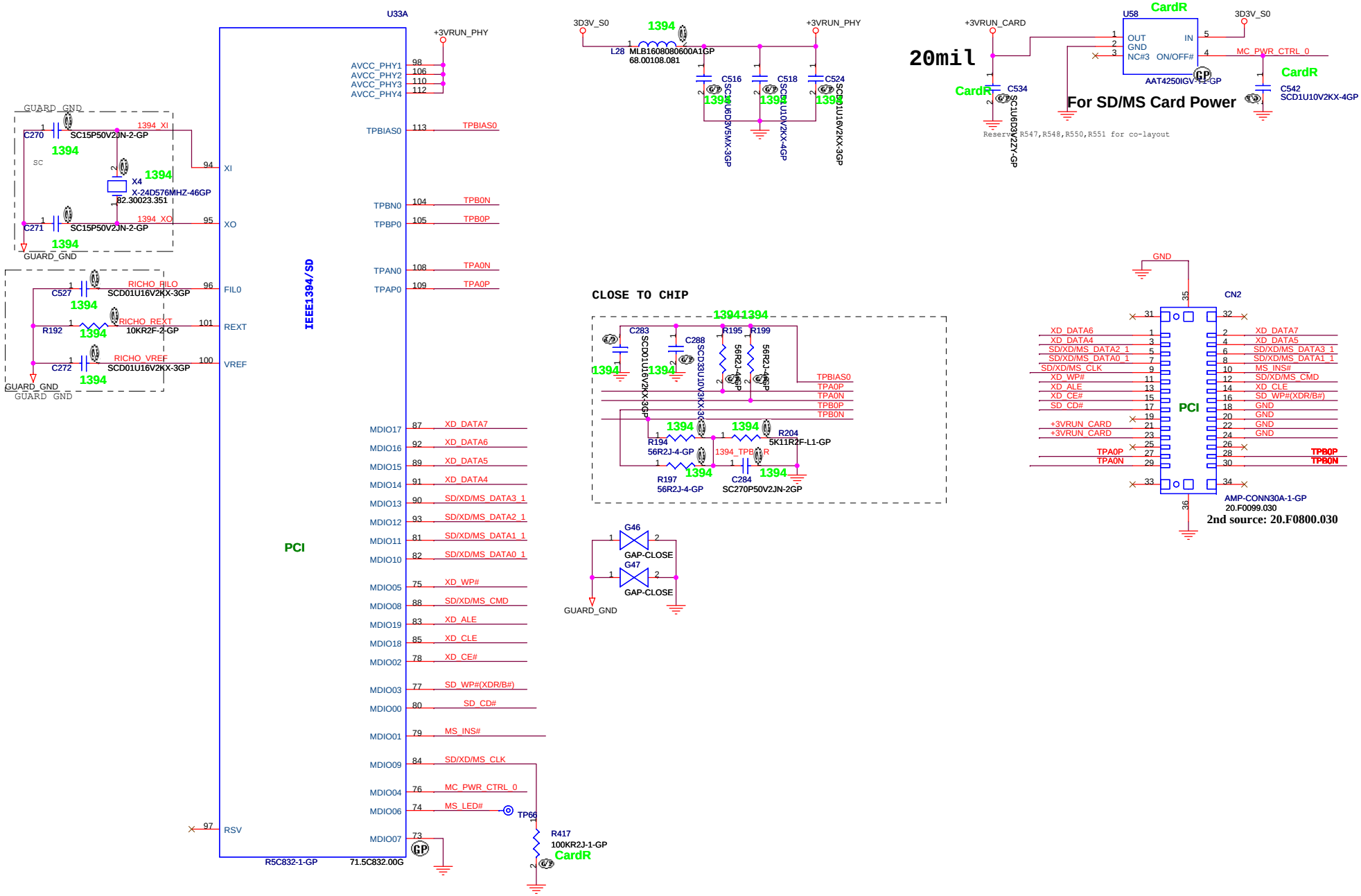
<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: R5C832_1394_7IN1(1/2)

Size	Document Number	Rev
A3	Garda5	SB

Date: Wednesday, April 26, 2006 Sheet 28 of 46



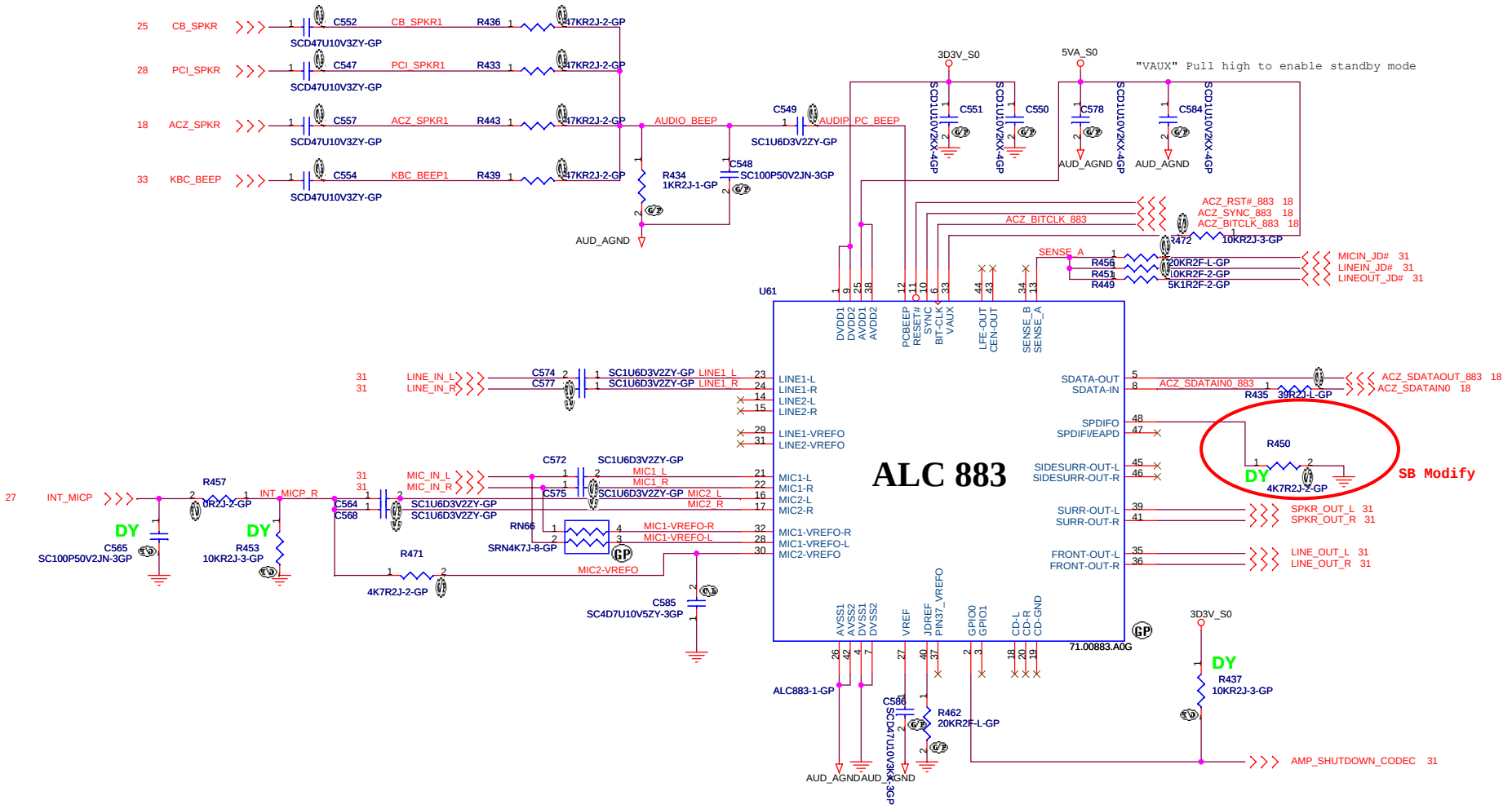
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

<Variant Name>

Title: R5C832_1394_7IN1(2/2)

Size: A3 | Document Number: Garda-5 | Rev: SA

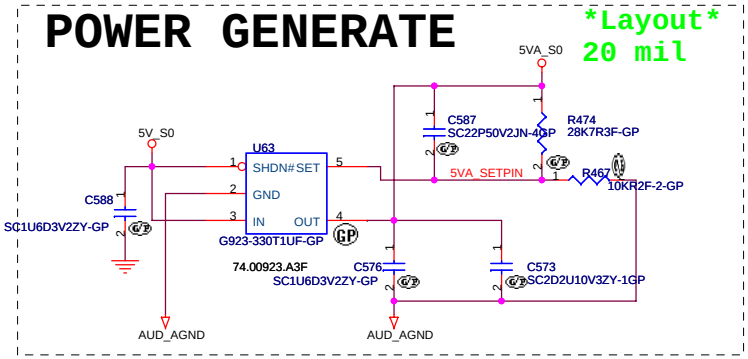
Date: Wednesday, April 26, 2006 | Sheet 29 of 46



1) When GPIO0 is assered, AMP should be muted.
2) SPDIFO should be turned off when not used.

Configuation:
(3 External Jacks, 1 internal Mic, 1 stereo output Speaker Amp.

Pin	Symbol	Location	Re-tasking
35/36	FRONT	AMP,Jack1	AMP output, line input
39/41	SURR	X	X
43/44	CEN/LEFT	X	SURR-VREFO-L/R
45/46	SIDESURR	X	SIDESURR-L is MIC2-VREFO-R, SIDESURR-R is LINE2-VREFO-R
23/24	LINE1	Jack 2	Line input, line output
21/22	MIC1	Jack 3	Mic input, line output
14/15	LINE2	X	X
16/17	MIC2	Int. Mic	Mic input



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

<Variant Name>

Title: Azalia codec ALC883

Size: A3 | Document Number: Garda-5 | Rev: SB

Date: Wednesday, April 26, 2006 | Sheet 30 of 46

AUDIO OP AMPLIFIER

I/P signal level need +5V level

Internal Speaker

SPKR_L-
SPKR_L+
SPKR_R-
SPKR_R+
SPKR1 ACES-CON4-1-GP
20.D0197.104
SRC100P50V-2-GP ERC2
2nd source: 20.F0760.004

EXT MIC IN

MICIN_JD#
MIC_IN_R
MIC_IN_L
R458 0R2J-2-GP MIC_IN_R_1
R459 0R2J-2-GP MIC_IN_L_1
EC84 SC100P50V3JN-2GP
EC85 SC100P50V3JN-2GP
EC86 SC100P50V2JN-3GP
MIC2
PHONE-JK233-GP
22.10133.B01

LINE OUT

SB Modify
LINEOUT_JD=lOW after PLUG-IN
LINEOUT_JD#
LINE_OUT_R_AMP
LINE_OUT_L_AMP
R447 33R2J-2-GP
R448 33R2J-2-GP
-1 Modify
RN65 SRN1KJ-7-GP
C555 SC680P50V2KX-2GP
C556 SC680P50V2KX-2GP
EC80 SC100P50V2JN-3GP
LOUT1
PHONE-JK235-GP
22.10133.B21
2ndsource: 22.10251.321
When has SPDIF replace to "22.10205.251".

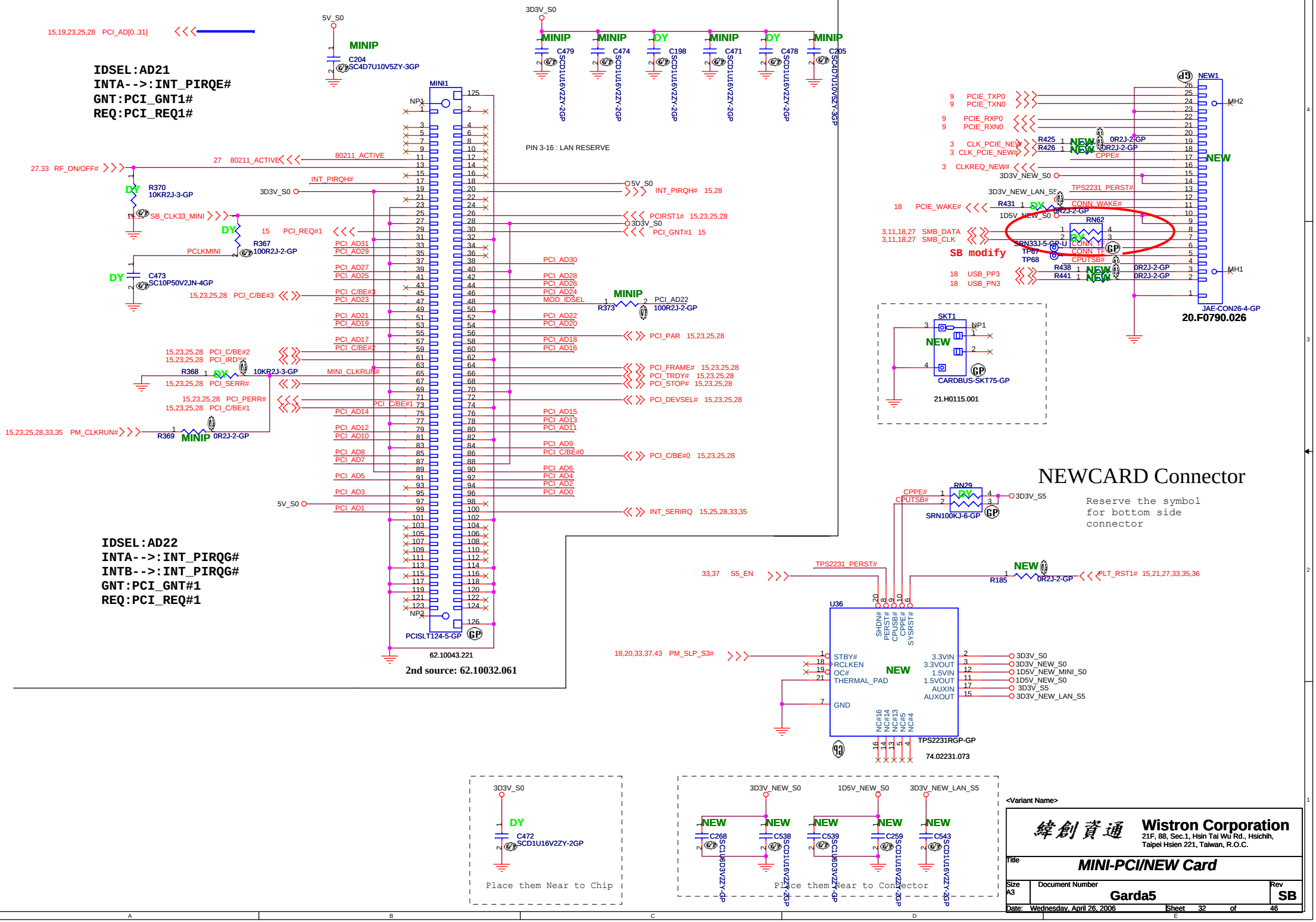
LINE IN

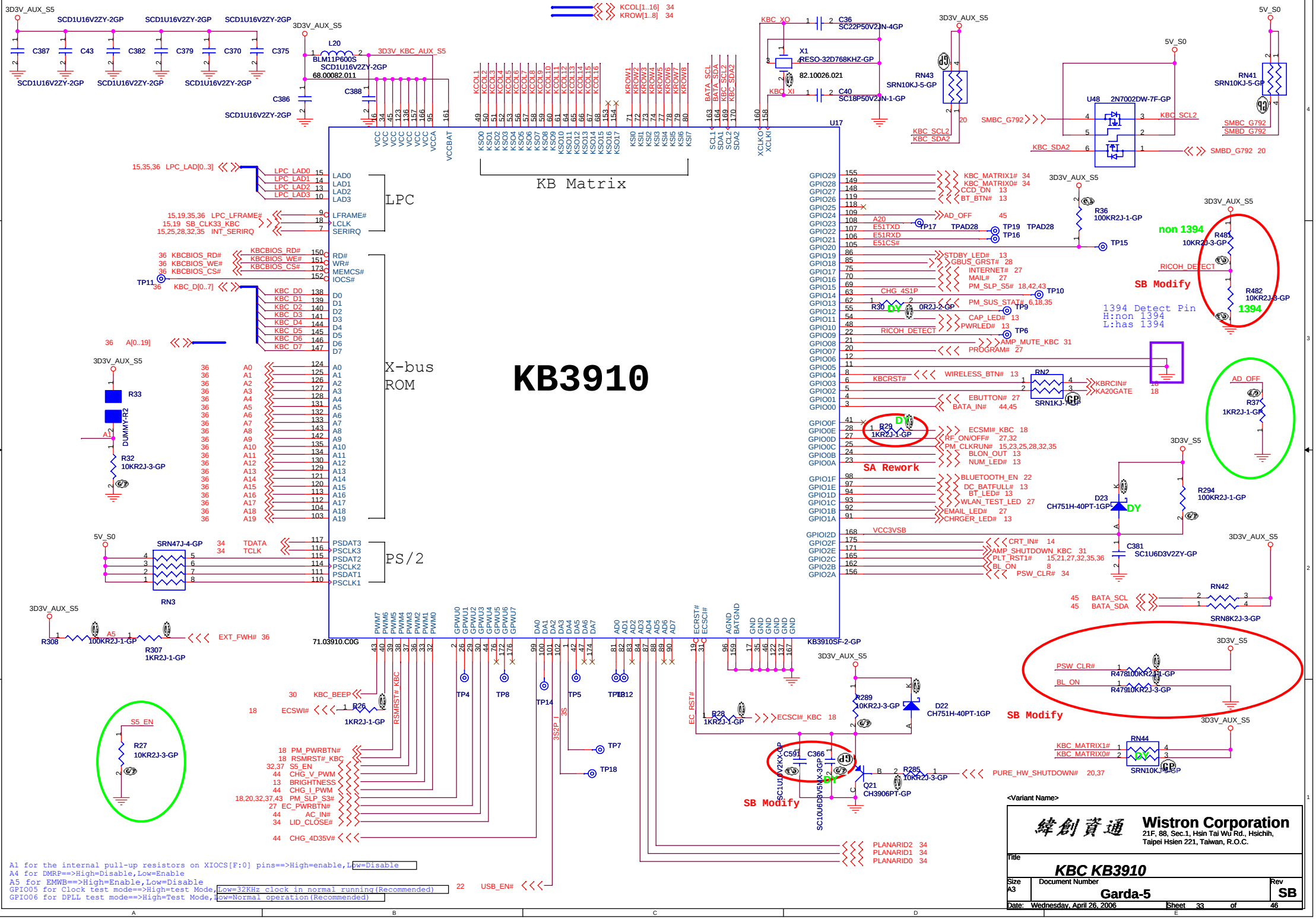
LINEIN_JD#
LINE_IN_R
LINE_IN_L
R454 0R2J-2-GP AUD_LINE_R
R455 0R2J-2-GP AUD_LINE_L
RN64 SRN10KJ-5-GP
EC83 SC100P50V2JN-3GP
EC82 SC100P50V2JN-3GP
EC81 SC100P50V2JN-3GP
PHONE-JK234-GP
LIN1
22.10133.B11

Key components and notes

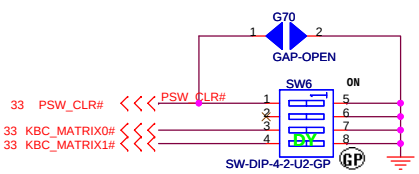
- U62 G1432Q5U-GP 74.01432.013
- U60 MAX4411ETP-1-GP 74.04411.A13
- SB Modify
- SA Modify
- DY
- -1 Modify
- 0.11 * 1.5 =0.165
- SB Modify FAE recommend
- MAX4411_PVSS

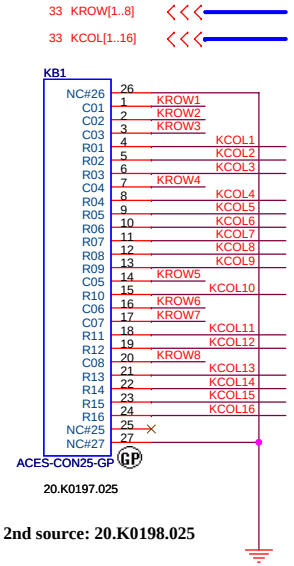
Wistron Corporation	緯創資通
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	AUDIO AMP AND JACK
Size A3	Document Number Garda-5
Rev	-1
Date: Wednesday, April 26, 2006	Sheet 31 of 46


IDSEL:AD21
INTA-->:INT_PIRQE#
GNT:PCI_GNT1#
REQ:PCI_REQ1#
IDSEL:AD22
INTA-->:INT_PIRQG#
INTB-->:INT_PIRQG#
GNT:PCI_GNT#1
REQ:PCI_REQ#1
MINI1
PCISLT124-5-GP
62.10043.221
2nd source: 62.10032.061
PIN 3-16 : LAN RESERVE
SB modify
NEWCARD Connector
Reserve the symbol for bottom side connector
JAE-CON26-4-GP
20.F0790.026
CARDBUS-SKT75-GP
21.H0115.001
TPS2231RGP-GP
74.02231.073
Place them Near to Chip
Place them Near to Connector
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
MINI-PCI/NEW Card
Garda5
Wednesday, April 26, 2006


KB3910
KB Matrix
LPC
X-bus ROM
PS/2
SB Modify
SA Rework
non 1394
1394 Detect Pin
H:non 1394
L:has 1394
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
KBC KB3910
Garda-5
Wednesday, April 26, 2006

Internal KeyBoard Connector





2nd source: 20.K0198.025

Keyboard matrix (from vendor)

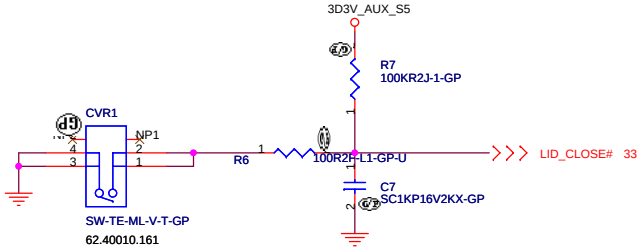
	US	Eur	Jap	Ohter
MATRIXID0#	1	0	1	0
MATRIXID1#	1	1	0	0

	Low Active
PSW_CLR#	1 - 5 ON
NC	2 - 6 ON
KBC_MATRIX1	3 - 7 ON
KBC_MATRIX2	4 - 8 ON

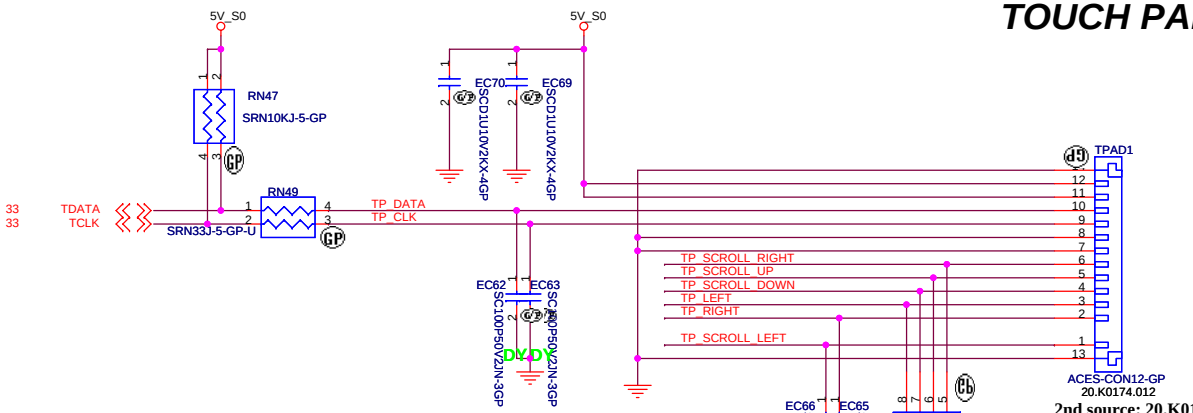
1 25

K/B

COVER SWITCH



TOUCH PAD

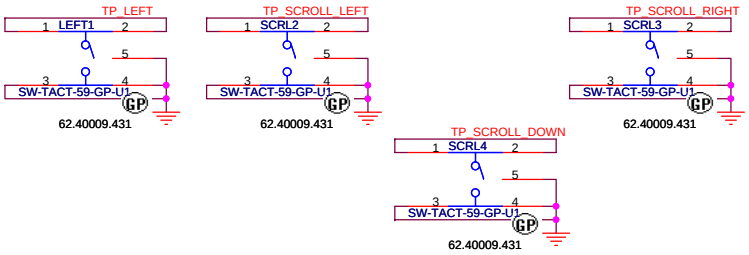


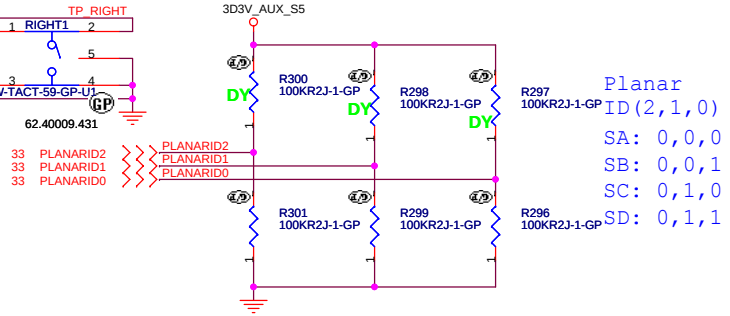
2nd source: 20.K0185.012

1 12

T/P

SCROLL KEY





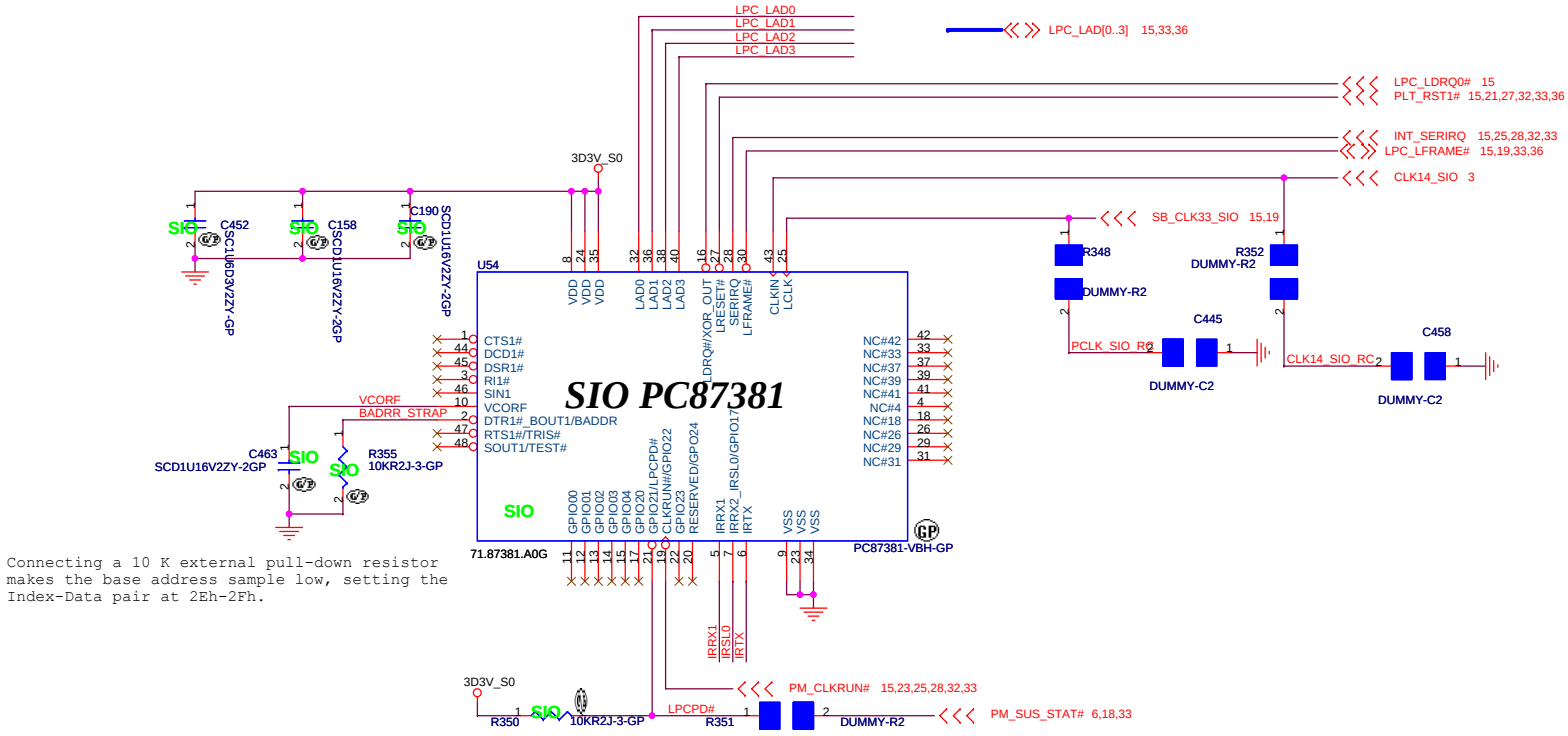
<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: KEYBOARD/TOUCHPAD

Size	Document Number	Rev
A3	Garda-5	SA

Date: Wednesday, April 26, 2006 Sheet 34 of 46

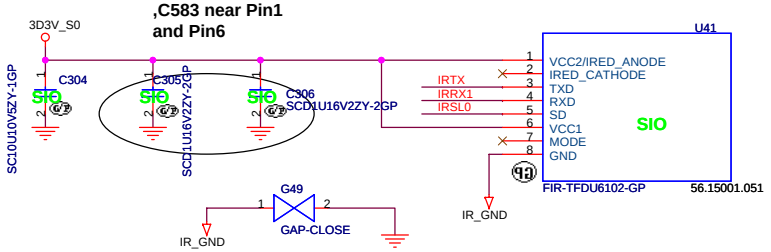


Connecting a 10 K external pull-down resistor makes the base address sample low, setting the Index-Data pair at 2Eh-2Fh.

VISHAY FIR/CIR Module

Place C581 ,C583 near Pin1 and Pin6

Layout Guide:
(1) FIR_3D3V : 30 mils,
(2) C583, C581 close to U32



<Variant Name>

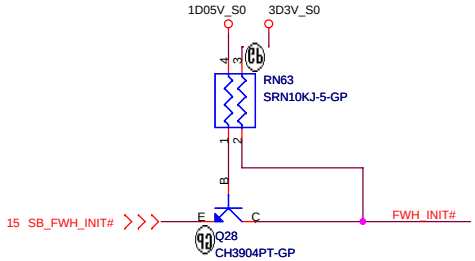
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

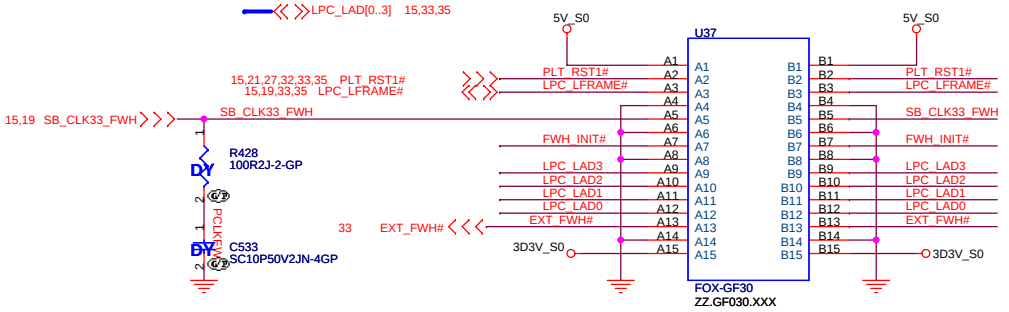
Title: **SIO 87381 / FIR**

Size: A3 | Document Number: **Garda-5** | Rev: **SA**

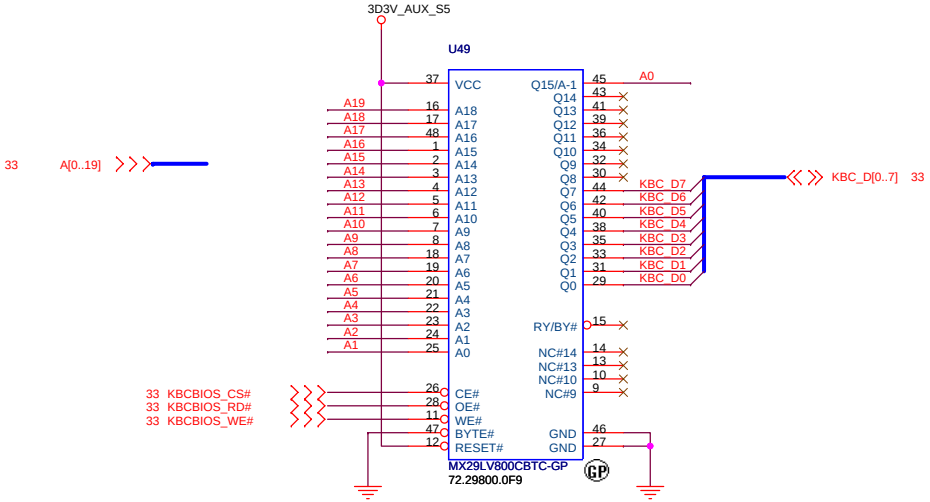
Date: Wednesday, April 26, 2006 | Sheet 35 of 46

GOLDEN FINGER FOR DEBUG BOARD





Boot Device must have ID[3:0] = 0000
Has internal pull-down resistors
All may be left floated
FPET7 Elec. P3-46



TOP VIEW

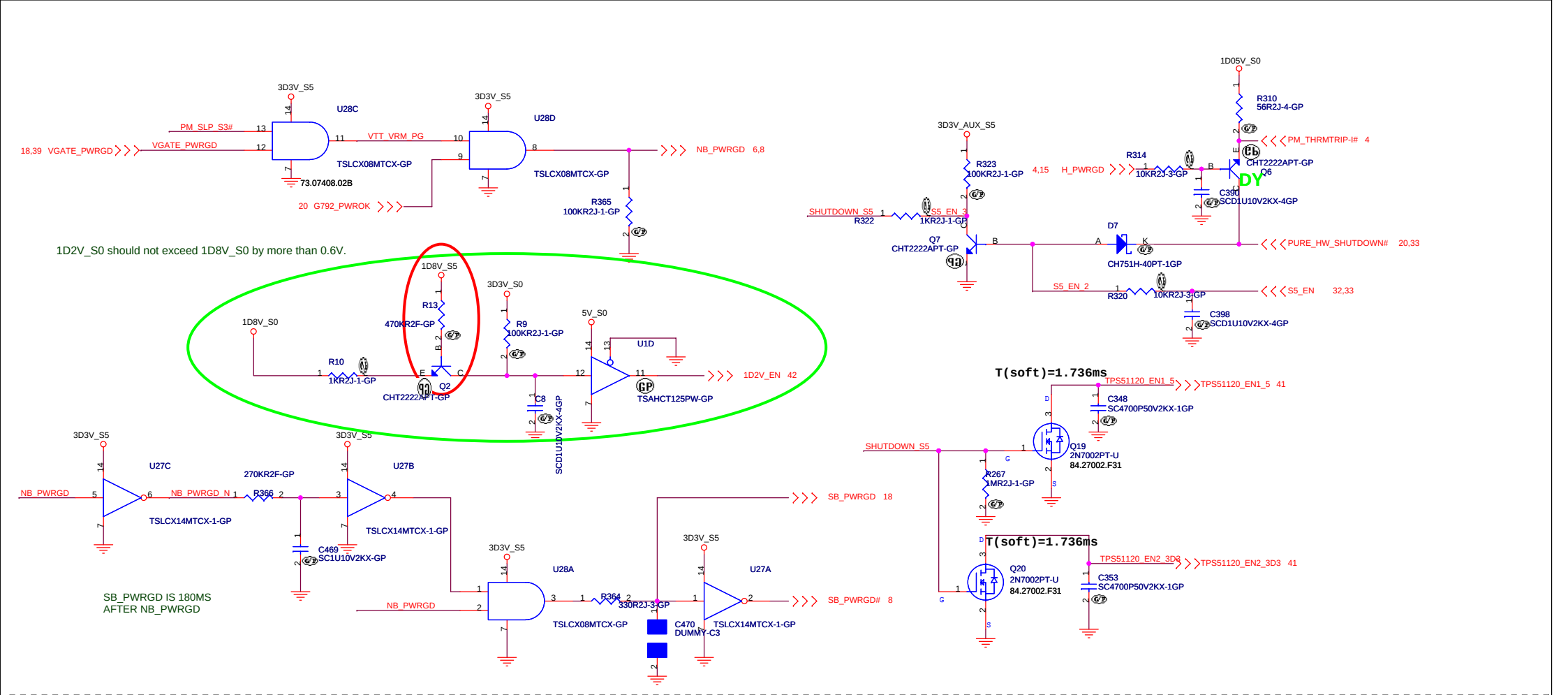
A15	(B1)
A14	(B2)
⋮	⋮
A2	(B14)
A1	(B15)

(BOTTOM VIEW)

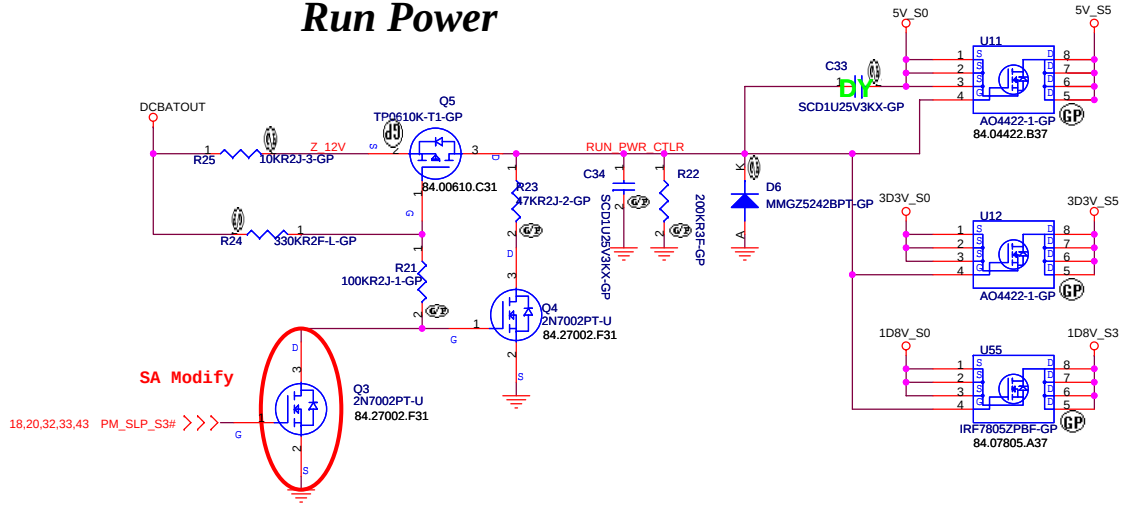
<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

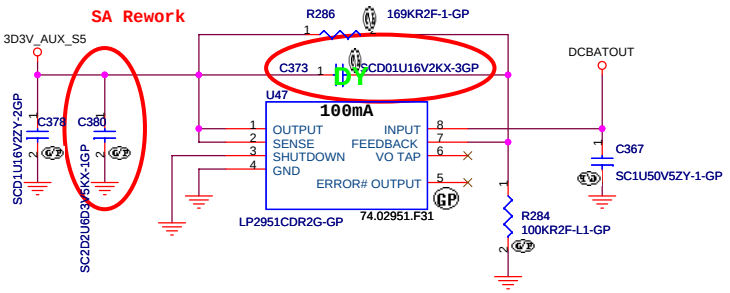
Title	***BIOS ROM***	
Size A3	Document Number **Garda-5**	Rev **SA**
Date: Wednesday, April 26, 2006	Sheet 36 of 46	



Run Power



Aux Power



<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **RUN and AUX POWER**

Size	Document Number	Rev
A3	Garda-5	SA

Date: Wednesday, April 26, 2006 Sheet 37 of 46

CPU_CORE
Intersil ISL6262

VID Setting
- H_VID0 → VID0(I / 1.05V)
- H_VID1 → VID1(I / 1.05V)
- H_VID2 → VID2(I / 1.05V)
- H_VID3 → VID3(I / 1.05V)
- H_VID4 → VID4(I / 1.05V)
- H_VID5 → VID5(I / 1.05V)
- H_VID6 → VID6(I / 1.05V)

Input Signal
- PSI# → PSI# (I / 3.3V)
- CPUCORE_ON → PGD_IN (I / 3.3V)
- PM_DPRSLPVR → DPRSLPVR (I / 3.3V)
- H_DPRSTP# → DPRSTP# (I / 3.3V)

Voltage Sense
- VCC_SENSE → VSEN(I / Vcore)
- VSS_SENSE → RTN(I / Vcore)

Input Power
- DCBATOUT_6262 → VCC(I)
- 5V_S0 → VCC(I)
- 3D3V_S0 → VCC(I)

Output Signal
- PGOOD(OD / 3.3V) → 6262_PWRGOOD
- CLK_EN#(O) → CLK_EN#

Output Power
- VCC_CORE_PWR(O) → VCC_CORE_S0(Imax=48A)

TPS51124
1D8V/1D05V

Input Power
- VCC ← 5V_S5
- VIN ← DCBATOUT_TPS51124

Input Signal
- EN1 ← TPS51124_EN1
- EN2 ← TPS51124_EN2

Output Signal
- PGOOD1 → CPUCORE_ON
- PGOOD2 → CPUCORE_ON

Output Power
- 1D8V (O) → 1D8V_S0 (7A)
- 1D05V(O) → 1D05V_S0 (7A)

CHARGER MAX8725

Input Signal
- ICTL ← CHGON#/OFF
- PKPRES ← BT_TH

Input Power
- ACIN ← AD+

Output Signal
- BATT → BT+SENSE
- ACOK → AC_IN

Output Power
- VOUT (O) → BT+
- VOUT (O) → DCBATOUT

TPS51120
5V/3D3V

Input Signal
- EN1 ← TPS51120_EN1_5
- EN2 ← TPS51120_EN2_3D3

Input Power
- VIN ← DCBATOUT_TPS51120

Output Signal
- PGOOD1(OD / 5V) → CPUCORE_ON
- PGOOD2(OD / 5V) → CPUCORE_ON

Output Power
- 5V(O) → 5V_DC_S5 (6A)
- 3D3V(O) → 3D3V_DC_S5 (5A)

Adapter

Input Signal (I)
- AD_OFF

Input Power
- VCC(I) ← AD_JK
- VCC(I) ← 5V_AUX_S5

Output Signal (O)
- AD_IN

Output Power
- VCC(O) → AD+

1D8V_S5
3D3V_S5 → INPUT / OUT → 1D8V_S5
APL5308-18DC-GP

1D5V_S0
3D3V_S5 → INPUT / OUT → 1D5V_CPU_S0
APL5312

1D5V_S0
3D3V_S5 → INPUT / OUT → 1D5V_NEW_MINI_S0
APL5332

1D05V_S0
1D2V_S3 → INPUT / OUT → 1D05V_S0
APL5912-KAC-GP

DDR_VREF_S0
5V_S5 → INPUT / OUT → DDR_VREF_S0
TPS51100DGQR-GP

3D3V_AUX_S5
DCBATOUT → INPUT / OUT → 3D3V_AUX_S5
LP2951ACM

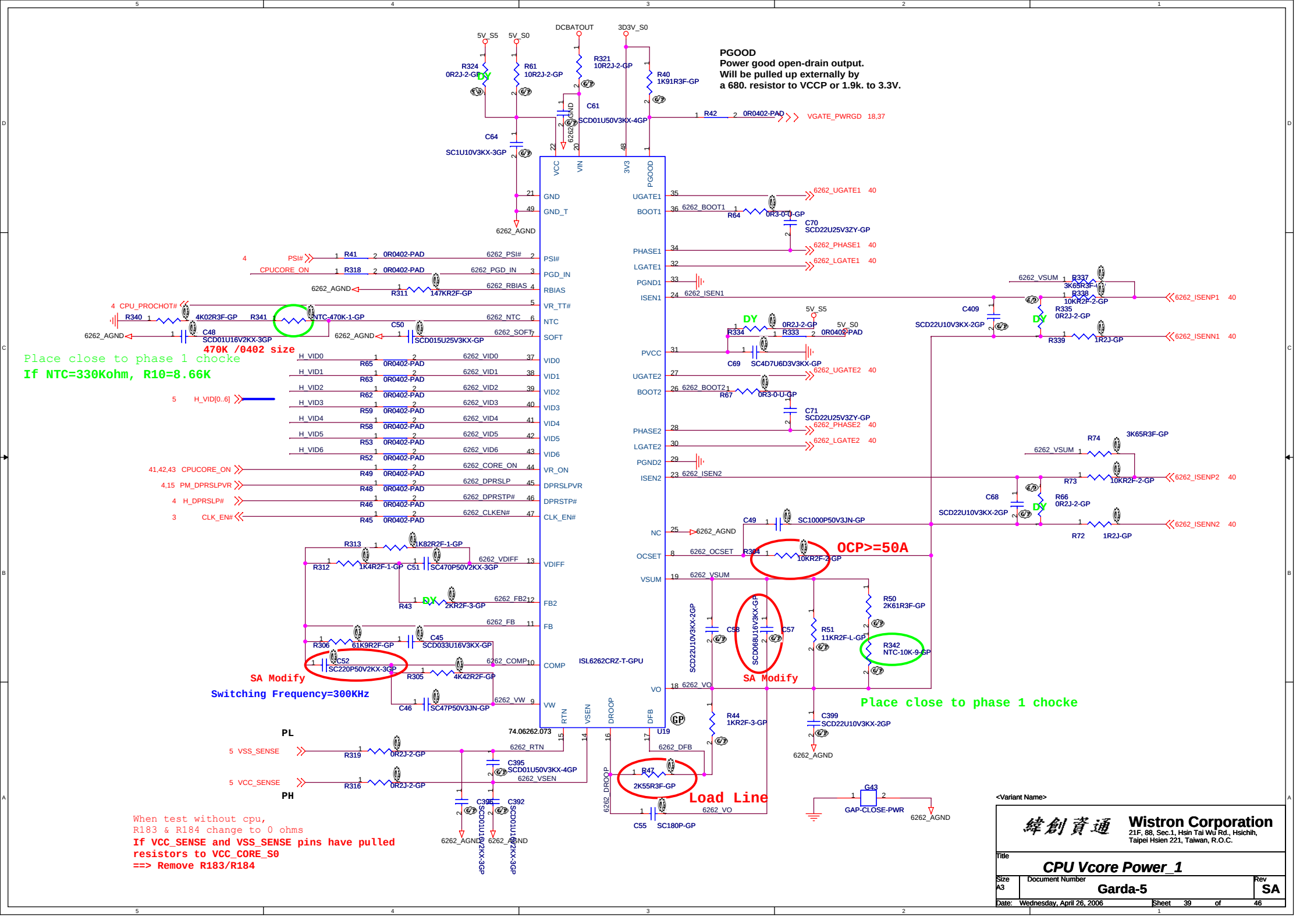
<Variant Name>

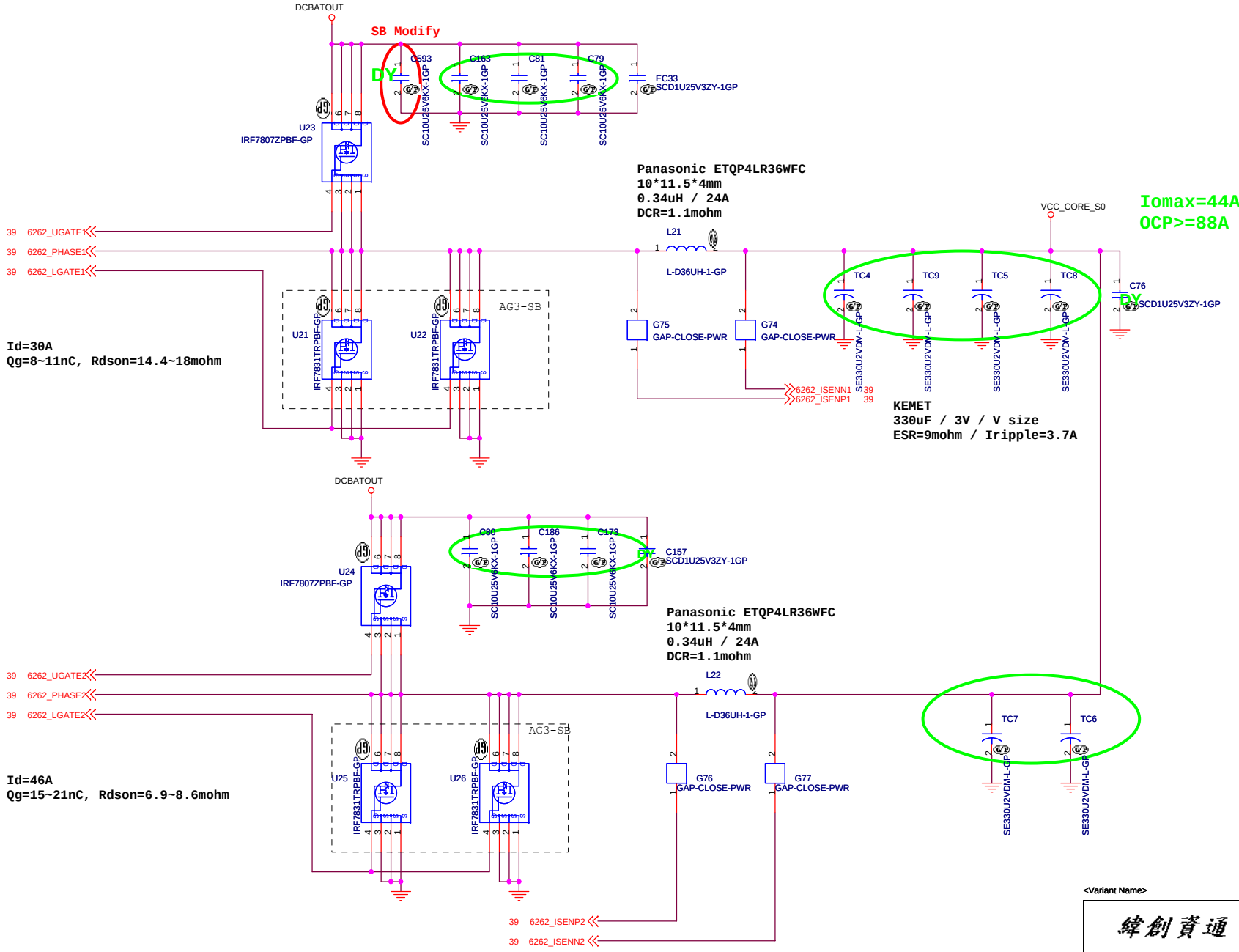
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **Power Block Diagram**

Size	Document Number	Rev
A3	Garda-5	SA

Date: Wednesday, April 26, 2006 Sheet 38 of 46


PGOOD
Power good open-drain output.
Will be pulled up externally by
a 680. resistor to VCCP or 1.9k. to 3.3V.
ISL6262CRZ-T-GPU
470K /0402 size
Place close to phase 1 chocke
If NTC=330Kohm, R10=8.66K
OCP>=50A
SA Modify
Switching Frequency=300KHz
Load Line
When test without cpu,
R183 & R184 change to 0 ohms
If VCC_SENSE and VSS_SENSE pins have pulled
resistors to VCC_CORE_S0
==> Remove R183/R184
PL
PH
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
CPU Vcore Power_1
Garda-5
Wednesday, April 26, 2006



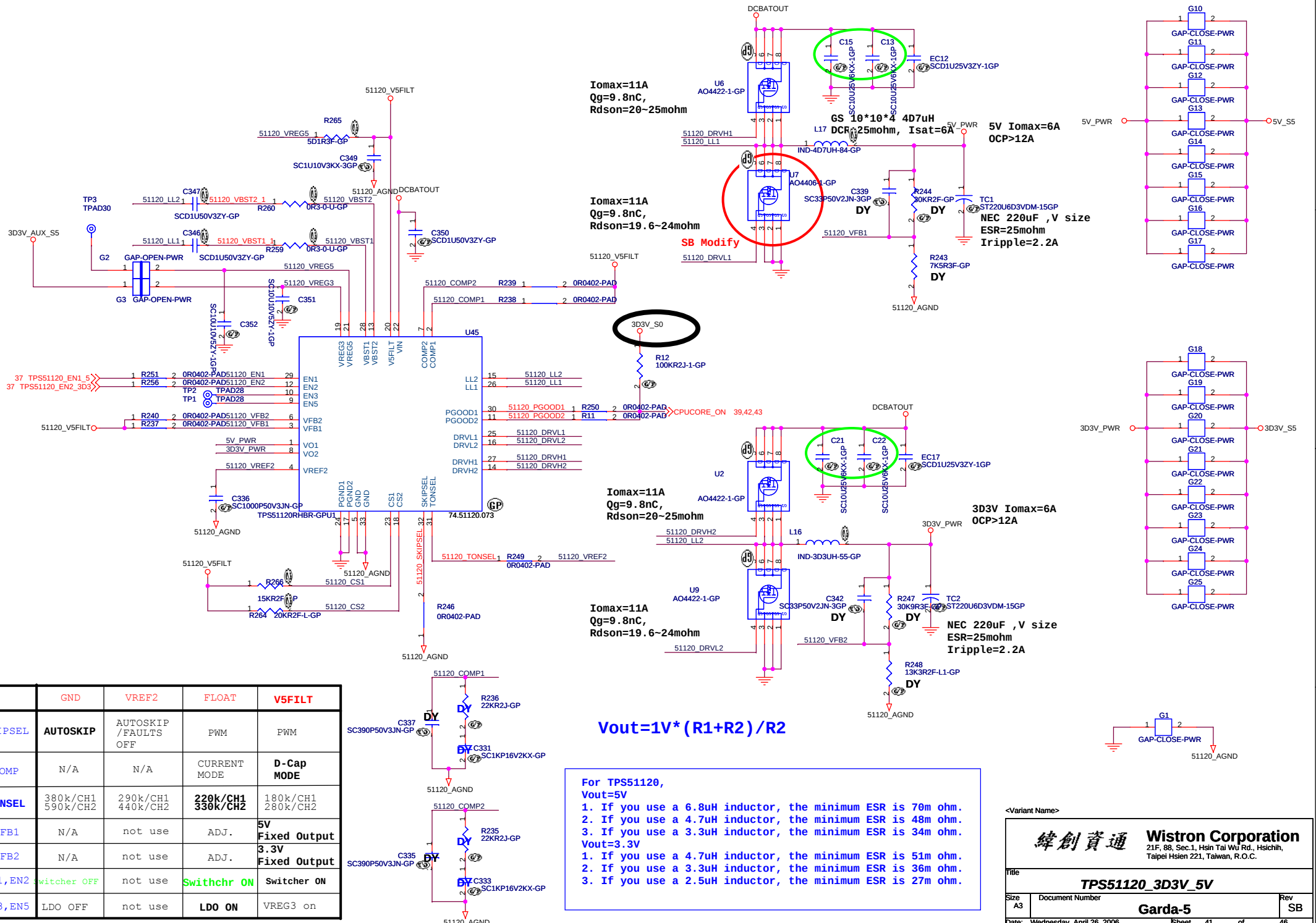
<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***CPU Vcore Power_2/2***

Size	Document Number	Rev
A3	Garda-5	SB

Date: Wednesday, April 26, 2006 Sheet 40 of 46



	GND	VREF2	FLOAT	V5FILT
SKIPSEL	**AUTOSKIP**	AUTOSKIP /FAULTS OFF	PWM	PWM
COMP	N/A	N/A	CURRENT MODE	**D-Cap MODE**
TONSEL	380k/CH1 590k/CH2	290k/CH1 440k/CH2	**220k/CH1 330k/CH2**	180k/CH1 280k/CH2
VFB1	N/A	not use	ADJ.	**5V Fixed Output**
VFB2	N/A	not use	ADJ.	**3.3V Fixed Output**
EN1,EN2	Switcher OFF	not use	**Swithchr ON**	**Switcher ON**
EN3,EN5	LDO OFF	not use	**LDO ON**	VREG3 on

For TPS51120,
Vout=5V
1. If you use a 6.8uH inductor, the minimum ESR is 70m ohm.
2. If you use a 4.7uH inductor, the minimum ESR is 48m ohm.
3. If you use a 3.3uH inductor, the minimum ESR is 34m ohm.

Vout=3.3V
1. If you use a 4.7uH inductor, the minimum ESR is 51m ohm.
2. If you use a 3.3uH inductor, the minimum ESR is 36m ohm.
3. If you use a 2.5uH inductor, the minimum ESR is 27m ohm.

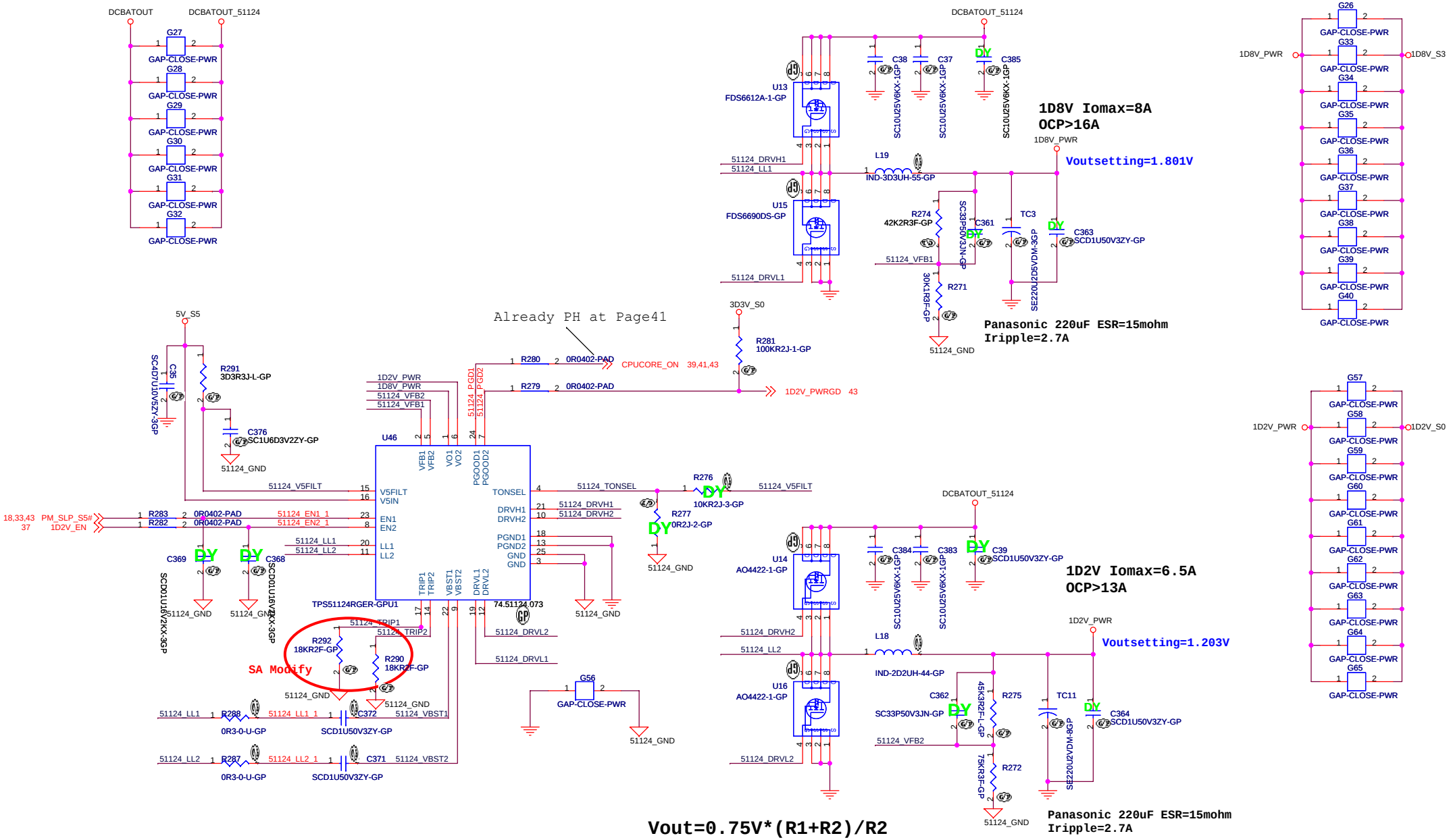
<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***TPS51120_3D3V_5V***

Size	Document Number	Rev
A3	**Garda-5**	SB

Date: Wednesday, April 26, 2006 Sheet 41 of 46



	GND	OPEN	V5FILT
TONSEL	230k/CH1 283k/CH2	283k/CH1 346k/CH2	346k/CH1 423k/CH2

<Variant Name>

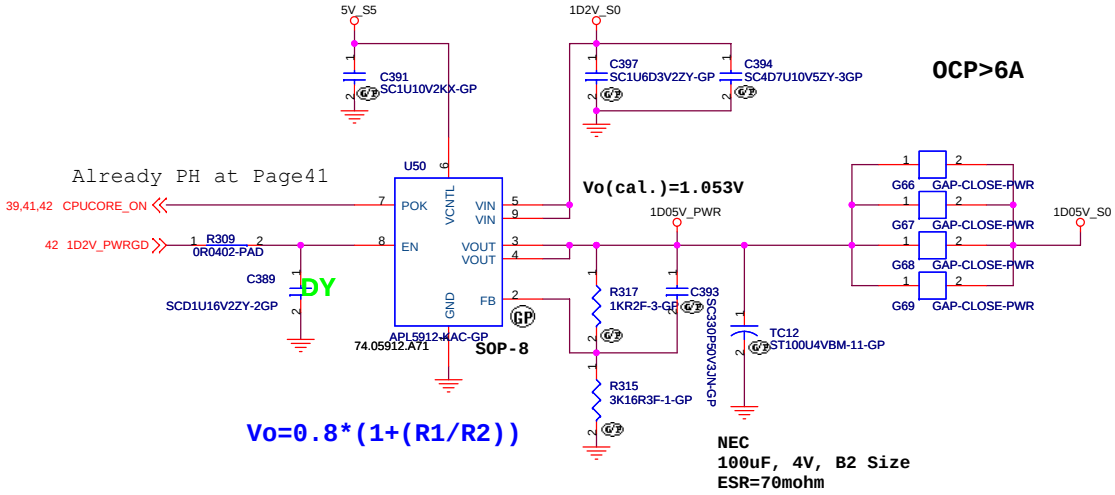
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS51124_1D8V_1D2V

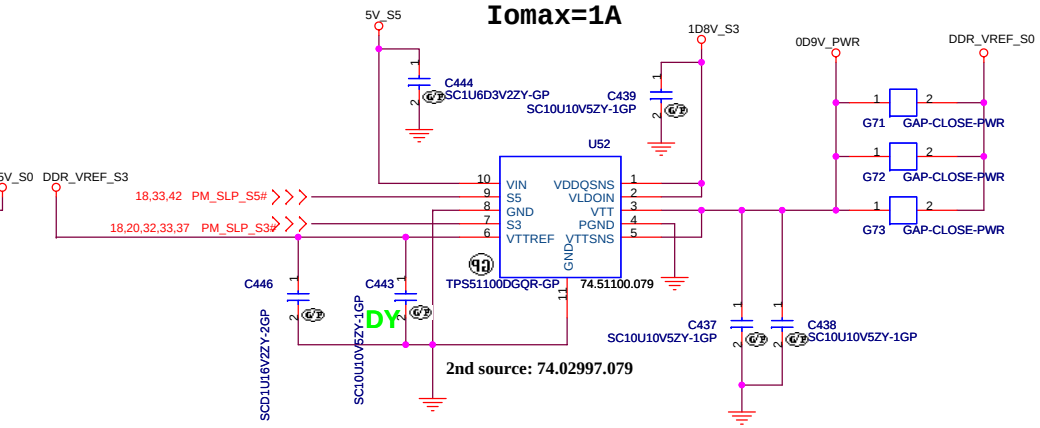
Size	Document Number	Rev
A3	Garda-5	SA

Date: Wednesday, April 26, 2006 Sheet 42 of 46

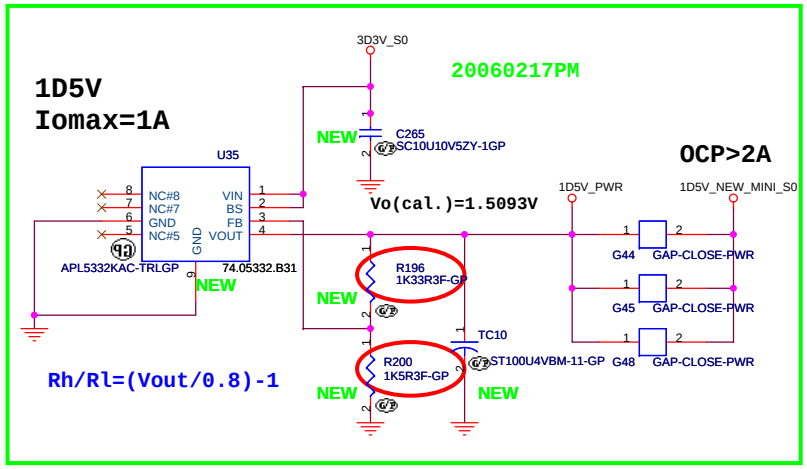
1D05V_S0
Iomax=3A



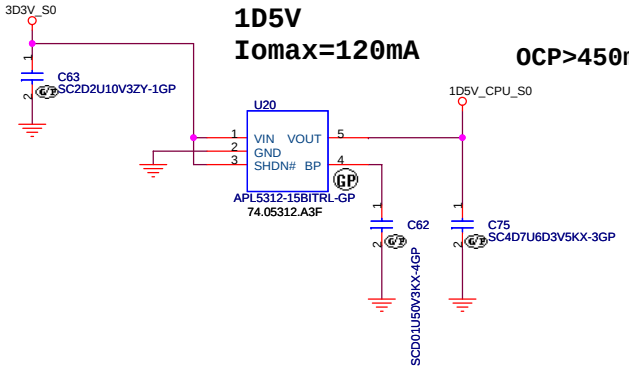
0D9V
Iomax=1A



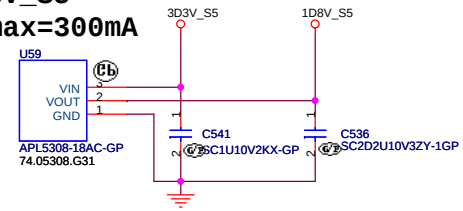
For New Card/MINI Card solution



1D5V
Iomax=120mA

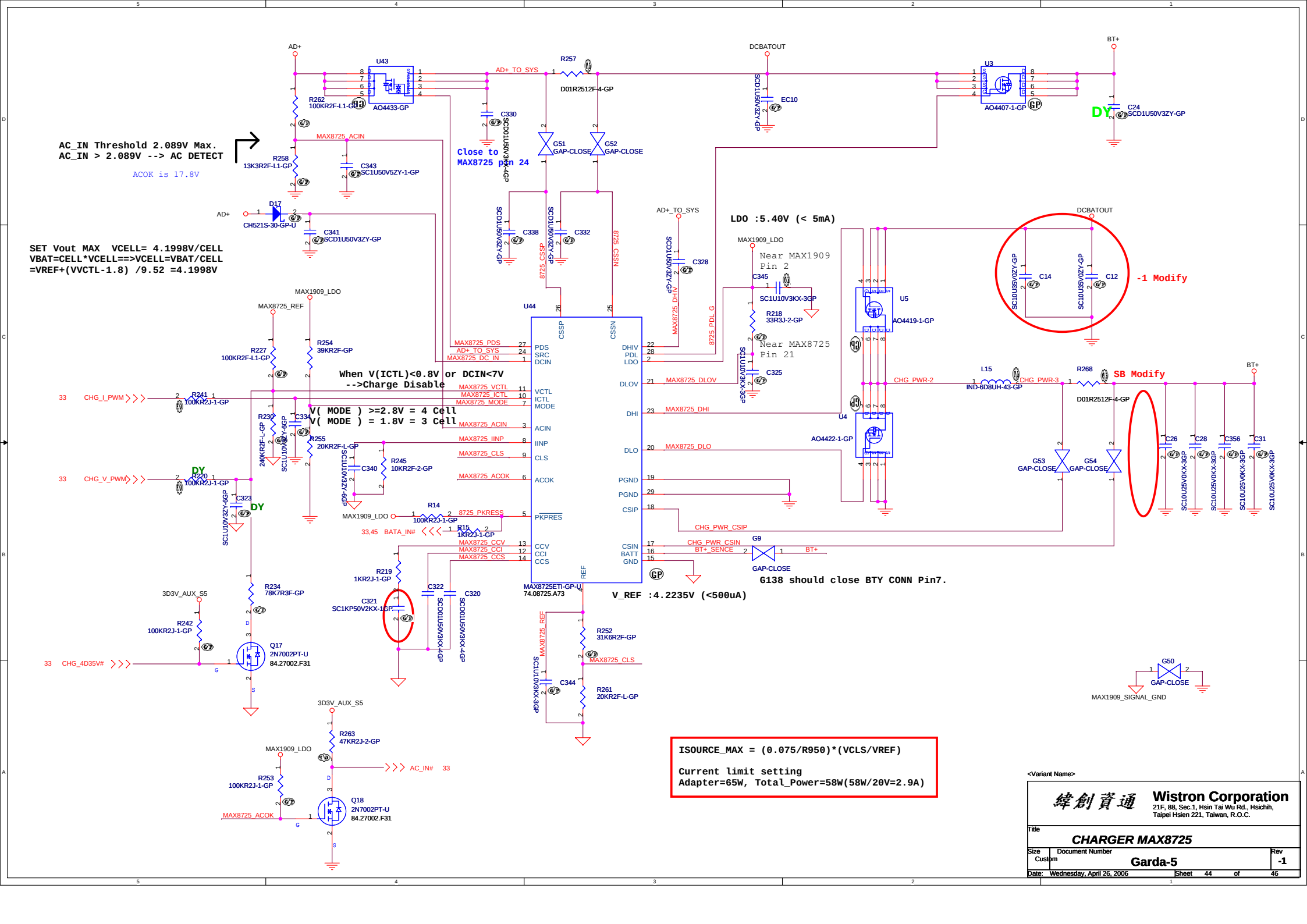


1D8V_S5
Iomax=300mA

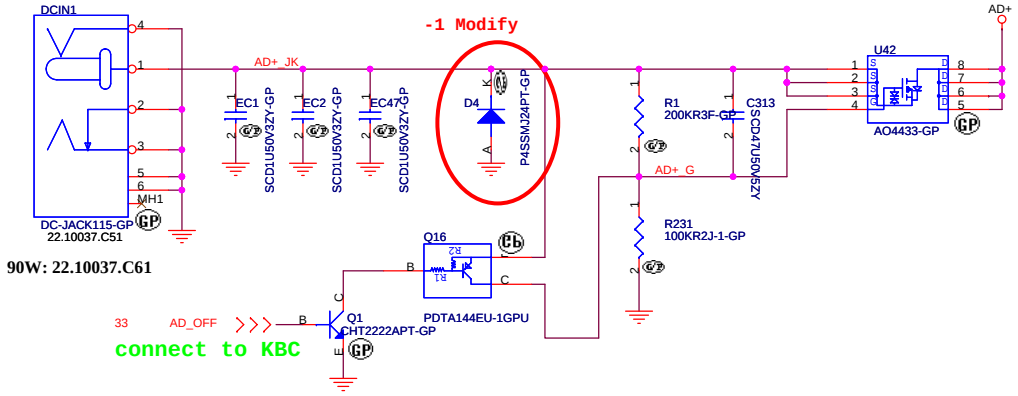


<Variant Name>

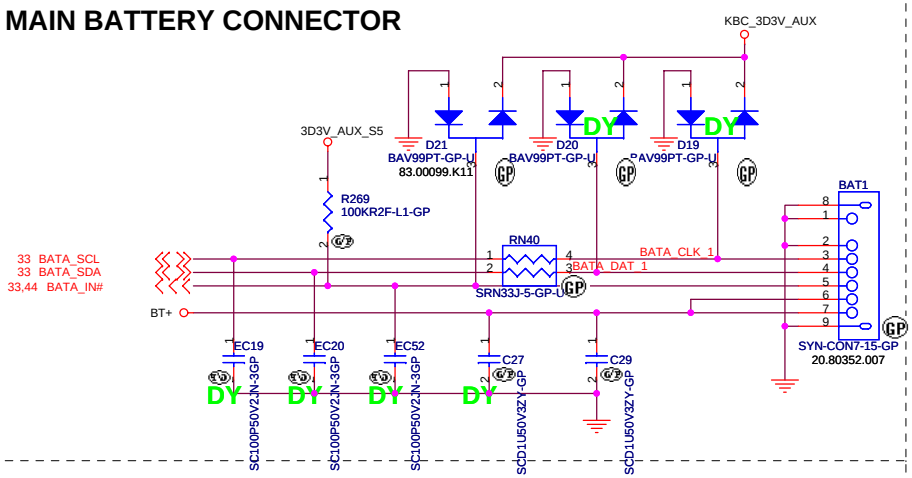
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: 1D5V/0D9V/1D05V/1D8V		
Size: A3	Document Number: Garda-5	Rev: SA
Date: Wednesday, April 26, 2006	Sheet 43 of 46	


AC_IN Threshold 2.089V Max.
AC_IN > 2.089V --> AC DETECT
ACOK is 17.8V
SET Vout MAX VCELL= 4.1998V/CELL
VBAT=CELL*VCELL==>VCELL=VBAT/CELL
=VREF+(VVCTL-1.8) /9.52 =4.1998V
When V(ICTL)<0.8V or DCIN<7V
-->Charge Disable
V(MODE) >=2.8V = 4 Cell
V(MODE) = 1.8V = 3 Cell
Close to MAX8725 pin 24
LDO :5.40V (< 5mA)
V_REF :4.2235V (<500uA)
G138 should close BTY CONN Pin7.
-1 Modify
SB Modify
ISOURCE_MAX = (0.075/R950)*(VCLS/VREF)
Current limit setting
Adapter=65W, Total_Power=58W(58W/20V=2.9A)
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
CHARGER MAX8725
Garda-5
Wednesday, April 26, 2006

ADAPTER IN CIRCUIT



MAIN BATTERY CONNECTOR



<Variant Name>

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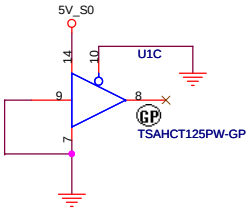
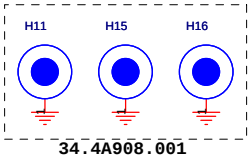
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	***AD/BATT CONN***	
Size: A3	Document Number: **Garda-5**	Rev: **-1**
Date: Wednesday, April 26, 2006	Sheet 45 of 46	

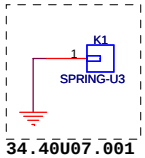


TOP SIDE:

CPU Thermal Module



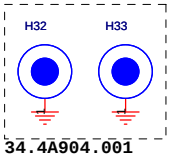
34.4A908.001



34.40U07.001

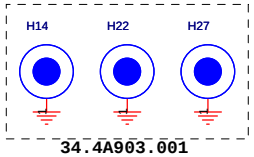
BOTTOM SIDE:

FOR Daughter BD

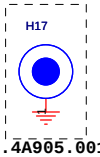


34.4A904.001

IO Bracket

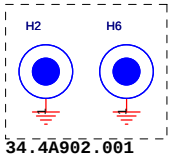


34.4A903.001



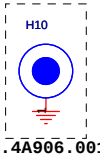
34.4A905.001

MDC



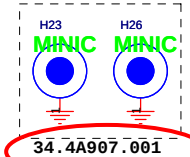
34.4A902.001

UMA



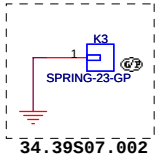
34.4A906.001

FOR MINIC



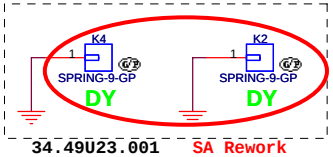
34.4A907.001

-1 Modify

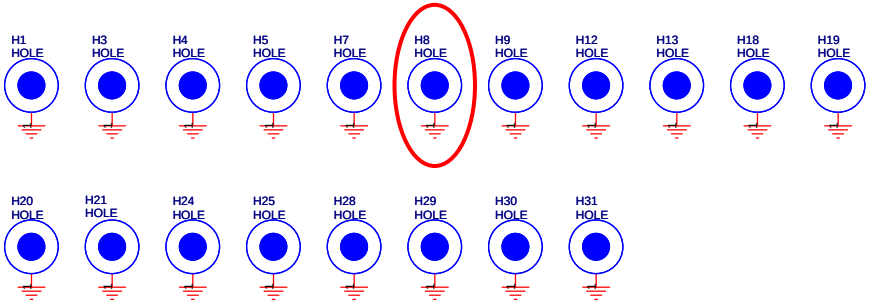


34.39S07.002

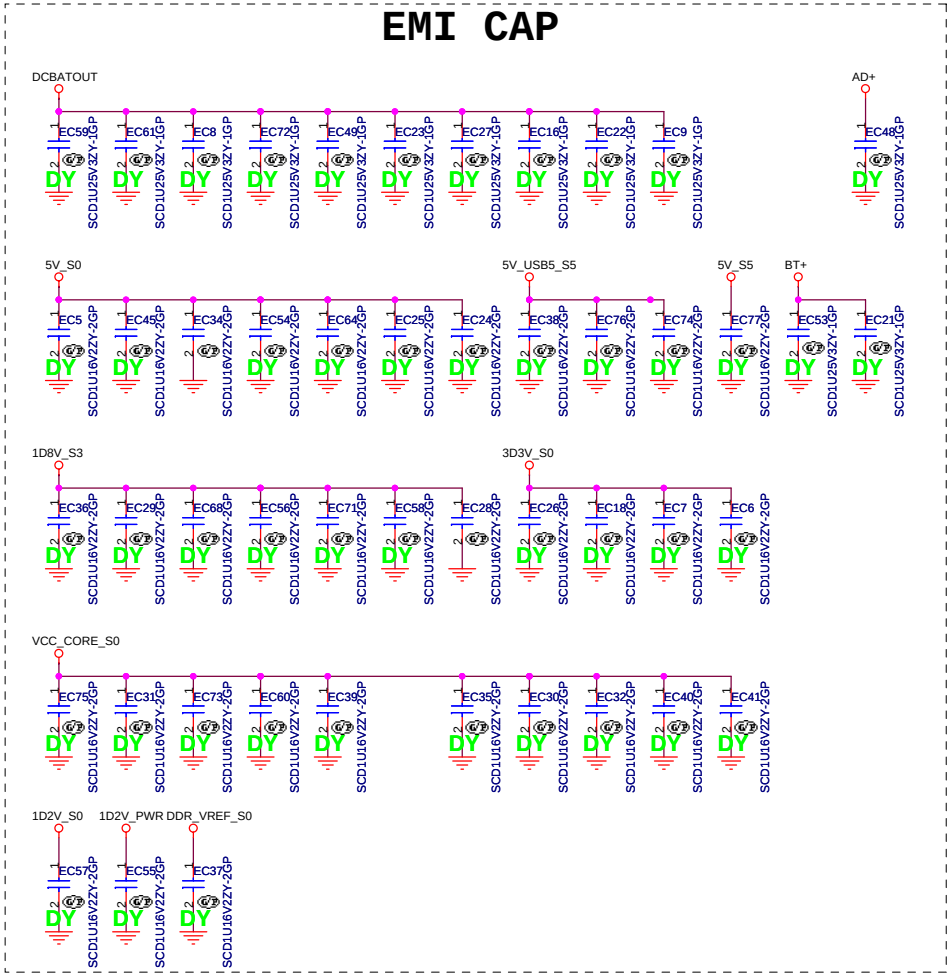
UNDER HDD



34.49U23.001 SA Rework



EMI CAP



<Variant Name>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: ***SPRING & BOSS***

Size	Document Number	Rev
A3	Garda-5	-1

Date: Wednesday, April 26, 2006 Sheet 46 of 46